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Readout system for the ATLAS end cap muon trigger chamber

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Abstract

A readout system for the ATLAS end cap muon trigger chamber has been developed. The system has a star architecture and a source synchronous serial communication is employed for the data path. FPGA modules are developed for prototyping and trial fabrication of ASIC is on going.

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Keywords: Readout system; Source-synchronous transmission; FPGA; ASIC

1. The ATLAS end cap muon trigger chamber

As an end cap muon trigger chamber for the ATLAS experiment, the thin gap chamber (TGC) is now under construction. A design study of the readout system for TGC is also on going. The TGC system consists of three stations of chambers, i.e. the inner, the middle triplet, and the middle doublet pair stations. Each station is divided into two regions, i.e., the end cap region and the forward region. The detail of the chamber system is given in Ref. [1]. The readout parameters are listed in Table 1 [2].

Requirements to the readout system are summarized as follows:

- The bandwidth of the data transfer path is moderate.
- The size of the chamber is so large that the propagation delay by the connecting cables are not negligible. Typical length of signal cables on the detector will be order 10 m.

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Table 1
TGC readout parameters. Number of LDBs (Local DAQ Blocks), boards, readout channels and data rates are listed. The letter F denotes the forward region and E denotes the end cap

	Per octant					
Station	LDBs	Slave Boards	No. Channels	Raw data (MB/s)	Encoded Hits/event	(kB/s)
Doublet F	1	21	2652	33.2	0.11	65.0
E	6	114	13 644	170.6	2.24	1342.0
Triplet F	1	18	1461	18.3	0.07	41.0
E	3	72	6612	82.7	0.57	344.2
Inner F	1	6	288	3.6	0.20	120.2
E	1	3	252	3.2	0.13	75.8
Total per octant	13	234	24 909	311.4	3.31	1988.2
Total 2 sides	208	3744	398 544	4981.8	53.02	31812.0

- Though the radiation environment is not so severe like inner detectors, still the so-called single-event effects should be taken care of.
- Although access to the chamber is not easy, some part of the electronics can be placed where relatively easier access can be obtained.

2. Readout system architecture

By analyzing the requirements, following basic architecture was proposed and the detailed design has started according to this scheme.

- Conventional serial communication of order 100 Mbps can be employed for the data path.
- A source synchronous transmission scheme should be used, where the data transfer timing is governed by, not the readout master (Local DAQ Master) but the data source front end modules (Slave Boards). Otherwise a strobe-acknowledge handshake is necessary which requires twice the total propagation delay on the cable connection.
- A star architecture is introduced. In this architecture, although an extra switch module (Star Switch) is necessary between the front end modules and the readout master, the connection between the front end and the switch becomes a simple point-to-point one, and the size of the protocol logic can be reduced considerably.

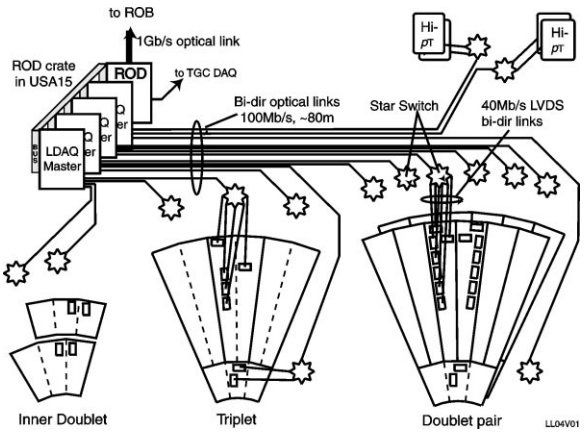

Fig. 1. Schematic diagram of the readout system architecture for the ATLAS TGC.

Schematic diagram of the readout system is shown in Fig. 1. Basically, the slave board has a level 1 (L1) pipeline buffer and, once the L1 trigger condition meets, the hit pattern in the L1 buffer is copied to the readout buffer named as a 'derandomizer' and is sent to the star switch via a serial transmission line. The switch has several sequencers inside and performs sparse data scan, formats the data before sending to the downstream local DAQ master.

Distance between the switch and the master is of order 80 m and a fiber-optic link will be used here.

3. Detailed design – technology choice

The design study of the slave boards, the star switch and the local DAQ master is in progress.

Slave board: A slave board receives the chamber signals. Two major functions are assigned to this module. One is to produce a trigger information on muon track candidates. The other is to keep hit data until the level 1 trigger is accepted and then to transmit them.

The core logic of this module will be fabricated as a gate array because the total number of chips will reach a few thousand and the radiation level is thought to be high at the location where these chips will be installed.

Star switch: The star switch will be implemented using FPGA devices, as the location of the switch modules will be at the edge of the muon chamber where the radiation level is expected to be relatively low. Recently the radiation tolerant FPGA products are also announced and related studies are done.

Local DAQ master: The local DAQ master sits apart from the experimental hall and there is no problem on radiation. Most updated technology will be introduced.

4. Prototyping

In order to verify the design, various prototyping studies are planned and performed.

- Computer simulation. Both analog and digital circuits are first verified by using simulation tools.

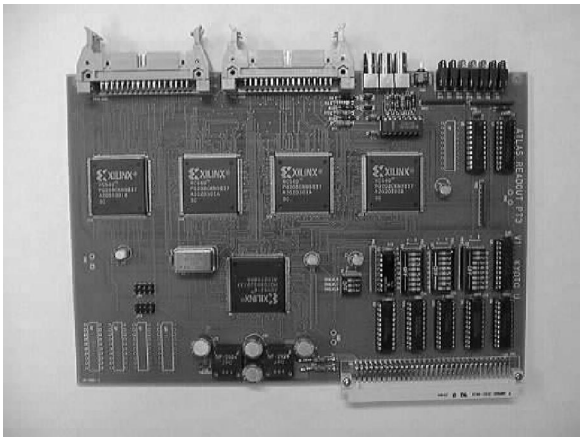

Fig. 2. Photograph of VME Field Programmable Gate Array (FPGA) module developed for prototyping of logic design.

- Verification by FPGA. Digital circuits are synthesized as an FPGA design and checked by using a VME FPGA module. Fig. 2 shows the module.
- Trial fabrication of Application Specific Integrated Circuit (ASIC). Using 0.6 μm full custom ASIC technology, main feature of the system is implemented and tested.

Design of the whole system is expected to be completed in year 2001 and then the mass production will start.

References

[1] ATLAS Muon Collaboration, ATLAS Muon Spectrometer Technical Design Report CERN/LHCC/97-22, 1997.
[2] ATLAS Level-1 Trigger Group, ATLAS Level-1 Trigger Technical Design Report, CERN/LHCC/98-14 ATLAS TDR 12, 1998.