Journal of Instrumentation

Design of a 32-channel NIM TDC module based on single FPGA for the μSR spectrometer prototype at the China Spallation Neutron Source

Jinst

Published by IOP Publishing for Sissa Medialab

Received: *March 28, 2019*
Accepted: *May 23, 2019*
Published: *June 3, 2019*

TECHNICAL REPORT

Design of a 32-channel NIM TDC module based on single FPGA for the μSR spectrometer prototype at the China Spallation Neutron Source

F.S. Deng,[a,b] **H. Liang,**[a,b,1] **J.Y. Tang**[c] **and B.J. Ye**[a,b]

[a] *State Key Laboratory of Particle Detection and Electronics (IHEP-USTC), University of Science and Technology of China (USTC), Hefei 230026, China*
[b] *Department of Modern Physics, University of Science and Technology of China (USTC), Hefei 230026, China*
[c] *Institute of High Energy Physics, Chinese Academy of Sciences, Beijing 100049, China*

E-mail: simonlh@ustc.edu.cn

Abstract: The design of an experimental muon source (EMuS) at the China Spallation Neutron Source (CSNS) has been underway for muon spin rotation, relaxation and resonance (μSR) experiments since 2007. A 128-channel μSR spectrometer prototype is also being developed. We have successfully developed a 32-channel time-to-digital converter (TDC) electronic readout unit module for the μSR spectrometer prototype. It receives timing signals from four front-end electronics (FEEs) and communicates with them. Moreover, it is a standard NIM module with a single field-programmable gate array-based design that meets the following requirements for μSR experiments: a low dead time, an instantaneous high count rate, a relatively long measurement duration, a relatively high resolution, and multiple channel-compatibility. By incorporating look-up tables (LUTs), placement constraints and area constraints, the routing skew of all TDC channels is reduced to less than 4 ps. Furthermore, Gigabit Ethernet data transmission has been incorporated in anticipation of more channels being added in the future.

Keywords: Data acquisition circuits; Instrumentation and methods for time-of-flight (TOF) spectroscopy; Modular electronics; Muon spectrometers

[1] Corresponding author.

https://doi.org/10.1088/1748-0221/14/06/T06002

2019 JINST 14 T06002

Contents

1 Introduction **1**
- 1.1 Design and implementation 3
- 1.2 32-channel TDC design 3
- 1.3 Gigabit Ethernet transmission 6
- 1.4 TDC module implementation 8

2 Test results and discussion **8**
- 2.1 DNL, INL and resolution 8
- 2.2 Dead time 10
- 2.3 Discussion 11

3 Conclusion **11**

2019 JINST 14 T06002

1 Introduction

The muon spin rotation, relaxation and resonance (μSR) technique [1, 2] plays an irreplaceable role in the study of the microstructure and properties of materials, especially the micro-magnetic properties. Currently only ISIS [3] in the U.K., J-PARC [4] in Japan, PSI [5] in Switzerland and TRIUMF [6] in Canada have high-performance muon sources for μSR application. To be able to carry out μSR experiments in China, an experimental muon source (EMuS) at China Spallation Neutron Source (CSNS) has been under development since 2007 [7–10]. A μSR spectrometer prototype is also being developed.

The μSR spectrometer prototype has 128 channels (64 front channels and 64 rear channels). It includes a collimator, a monitor, an external magnetic field, a sample chamber and photomultiplier tube (PMT) detectors, as shown in figure 1. The integrated design has been completed and the model is shown in figure 2 [10]. A pulsed muon beam is injected into the sample; then, the muon will rapidly decay to produce a large number of positrons ($\mu^+ \rightarrow e^+ + \nu_e + \nu_\mu$), which are detected by PMTs. The period between the time that the muon beam passes through the monitor (start) and the time that the positrons are received by the detectors (stops) is what we need to measure. The key information of the sample can be obtained by analysing this time spectrum. Therefore, time measurement is the key to the entire μSR spectrometer prototype.

μSR experiments mandate some specific requirements for time measurement. Because muon decay produces a large number of positron events, a time-to-digital converter (TDC) needs to have a hit buffer that is capable of storing large amounts of data. Furthermore, because most of the positrons are generated in the early phase of muon decay, theoretically, a shorter dead time is better. However, the typical recovery time of a PMT is approximately 20 ns, and the recovery time of an avalanche photodiode (APD) is even longer (approximately 40 ns). Therefore, the dead time of the TDC must be less than 20 ns. Although the mean lifetime of muon is 2.2 μs, the measurement duration needs

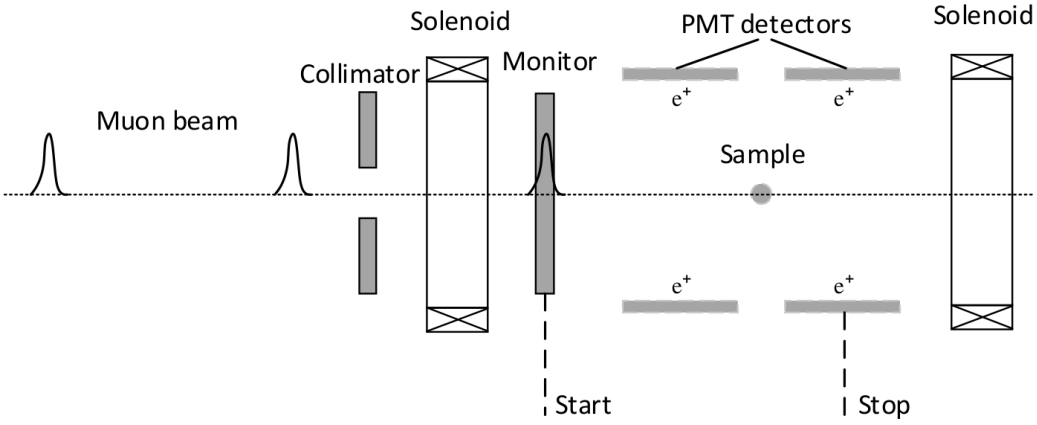

Figure 1. Schematic of the μSR spectrometer prototype.

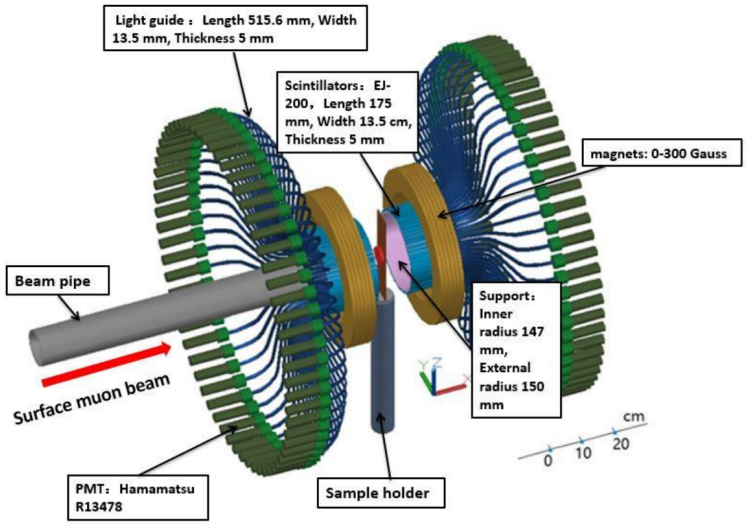

Figure 2. Model of the μSR spectrometer prototype.

to be much longer to ensure that no events are lost; generally, it exceeds 32 μs. In addition, the time resolution should not be too low. J-PARC demonstrated the PMT-based μSR spectrometer and silicon photomultiplier (SiPM)-based μSR spectrometer to have a time resolution of 1 ns in 2009 and 2014, respectively [11, 12]. Owing to the low count rate per channel, μSR spectrometers often have many channels. Even if the dead time is 20 ns and the positrons arrive uniformly within 2.2 μs, the count per channel is only 2.2 μs / 20 ns = 110 counts/pulse. Considering that the repetition rate of EMuS is 2.5 Hz, the average count rate per channel is less than 275 counts/s.

Although there are many commercial TDC chips, it is difficult to find a TDC chip that meets the requirements for μSR experiments (i.e., a dead time of less than 20 ns, number of hits that exceeds 110, measurement duration of more than 32 μs, resolution of less than 1 ns, and number of channels that exceeds 16). Some TDC chip parameters are listed in table 1. Commonly used TDC chips (TDC-GP22 and TDC-GP21) do not meet the requirements for the number of hits, measuring duration and number of channels. Although the AS6501 and TDC-GPX2 exhibit good overall

2019 JINST 14 T06002

Table 1. Various TDC Chip Parameters.

Name	Dead time	Number of hits	Measuring duration	Resolution	Number of channels
TDC-GP22	20 ns	4	3.5 ns to 2.4 µs	90 ps	2
TDC-GP21	20 ns	4	3.5 ns to 2.5 µs	90 ps	2
TDC-GP30	—	31	10 µs to 4096 µs	11 ps	2
AS6501	5 ns	Unlimited	0 s to 16 s	10 ps	2
TDC-GPX2	5 ns	Unlimited	0 s to 16 s	10 ps	4

performance, the number of channels in each chip is too low. This causes integration and price to become significant concerns. Data transmission is also a factor that needs to be considered.

Taking these factors into consideration, we developed an electronic readout unit for 32-channel TDC module. The 32-channel TDC and Gigabit Ethernet data transmission are implemented in a single Xilinx Virtex-6 field programmable gate array (FPGA). The dead time of the TDC is less than 10 ns, and the maximum hit buffer storage is 512. The measuring duration ranges from 0 to 327.68 µs, and the RMS time resolution is less than 184.7 ps. This TDC module also controls four 8-channel front-end electronics (FEEs), which are used to convert the detector signals into timing pulses.

1.1 Design and implementation

1.2 32-channel TDC design

To meet the requirements for µSR experiments, while also minimizing the cost incurred by implementing a high channel count, we employed a multi-phase clock sampling method to reduce the consumption of logic resources, thereby preserving sufficient resources for data buffering, Gigabit Ethernet logic and control logic. Xilinx Virtex-6 FPGA (xc6vlx240t-2ff1156) has 32 global clock lines, but only 12 global clock lines can be routed in one region. In this design, the external 100-MHz clock is multiplied by a clock-generating IP core to generate eight 200-MHz clocks that operate on the same frequency, with a 50% duty cycle, but have a phase difference of 22.5 degrees between neighbouring clocks. The input signal of each channel is routed to 16 flip-flops (FFs), with eight FFs being activated by the rising edges of the eight clocks and the other eight FFs being activated by the falling edges of the eight clocks. This is equivalent to the input signal being sampled by 16 equidistant phase-shifted 200-MHz clocks. The TDC bin size is Tclk/N, where Tclk is the clock sampling period, and N is the number of sampled clocks. Thus, the bin size is 312.5 ps; however, it can be further improved by increasing the clock frequency if necessary.

Since there is no equal-length constraint for the FPGA, the time skew of input signal that is routed to the sampled FFs most critically affects the resolution. To minimize the routing skew, the look-up tables (LUTs) were incorporated, as shown in figure 3. The input signal is routed to 16 FFs after four stages of LUTs and these LUTs are symmetrically positioned in a single-slice column, with only one LUT in each slice [13]. We designed the output of each LUT to equal its input by configuring each LUT. Symmetrical placement of the LUT brings the route lengths closer. There are four LUTs in each slice, thus we can always find the LUT with the smallest routing skew. Table 2 shows the details of a typical routing skew provided by the ISE Design Suite; the skew is in the range of 0 ps to 4 ps. However, this is only the result obtained under ideal conditions. Owing to the

2019 JINST 14 T06002

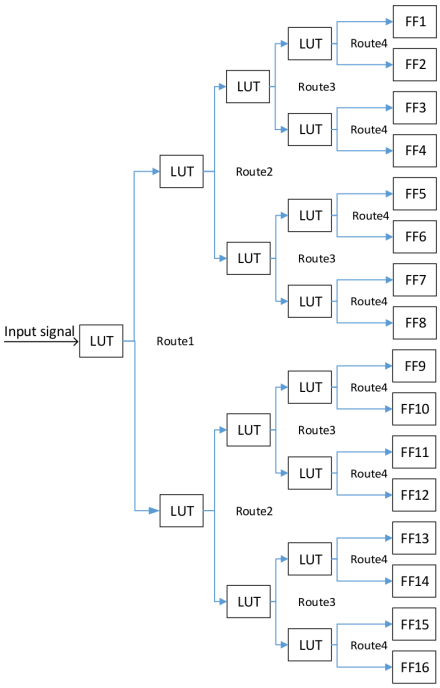

Figure 3. Routing skew is minimized by inserting LUTs.

automatic layout and routing of other parts of the logic, a few optimal routings are always occupied; this significantly increases the routing skew. To ensure that the configurable logic blocks (CLBs) where these LUTs and FFs are located are not occupied, we imposed area constraints on other parts of the logic, as shown in figure 4. The LUTs and FFs of the 33 TDC channels, including one start channel and 32 stop channel, are positioned in the upper and lower left corners, and other parts of the logic are constrained in other areas. As a result of this configuration, the routing skew of all channels is in the range of 0 to 4 ps; therefore, the routing skew does not limit the resolution of the multi-phase clock sampling-based TDC.

Because the input signal is sampled by the 16 FFs, the information of which is distributed amongst several phase-shifted clocks, it needs to be synchronized to the same clock domain for encoding. To minimize the setup time, only the sampled data of two neighbouring phase-shifted clocks are sequentially synchronized in each clock cycle, and after 15 clock cycles, all of the sampled data are synchronized to the same clock domain, as shown in figure 4. The minimum setup time is $(N-1)/N \times$ Tclk, where N represents the number of phase-shifted clocks. This configuration significantly reduces the routing difficulty.

The structure of the 32-channel TDC is shown in figure 5. It includes a start channel and 32 stop channels, which are respectively connected to the outputs of the monitor and the 32 PMTs. The input signal of each channel is routed to 16 FFs driven by 16 phase-shifted 200-MHz clocks with minimal time skew. The sampled data of the FFs are encoded into 4-bit binary code as a fine count after being synchronized with one 200-MHz clock domain. With each start event, the 16-bit coarse counter is reset and restarts counting until the maximum value is reached. When stop event occurs, the two fine counts (start and stop) and the coarse count are transmitted to the 20-bit

2019 JINST 14 T06002

Table 2. Typical routing skew provided by the ISE Design Suite. (Remarks: R1, R2, R3 and R4 correspond to Route1, Route2, Rout3 and Route4 in figure 3, respectively.)

Name	R1/ps	R2/ps	R3/ps	R4/ps	Total/ps	Skew/ps
Input to FF1	527	364	353	316	1560	0
Input to FF2	527	364	353	316	1560	0
Input to FF3	527	364	353	316	1560	0
Input to FF4	527	364	353	316	1560	0
Input to FF5	527	363	352	316	1558	−2
Input to FF6	527	363	352	316	1558	−2
Input to FF7	527	363	352	316	1558	−2
Input to FF8	527	363	352	316	1558	−2
Input to FF9	525	364	353	316	1558	−2
Input to FF10	525	364	353	316	1558	−2
Input to FF11	525	364	353	316	1558	−2
Input to FF12	525	364	353	316	1558	−2
Input to FF13	525	363	352	316	1556	−4
Input to FF14	525	363	352	316	1556	−4
Input to FF15	525	363	352	316	1556	−4
Input to FF16	525	363	352	316	1556	−4

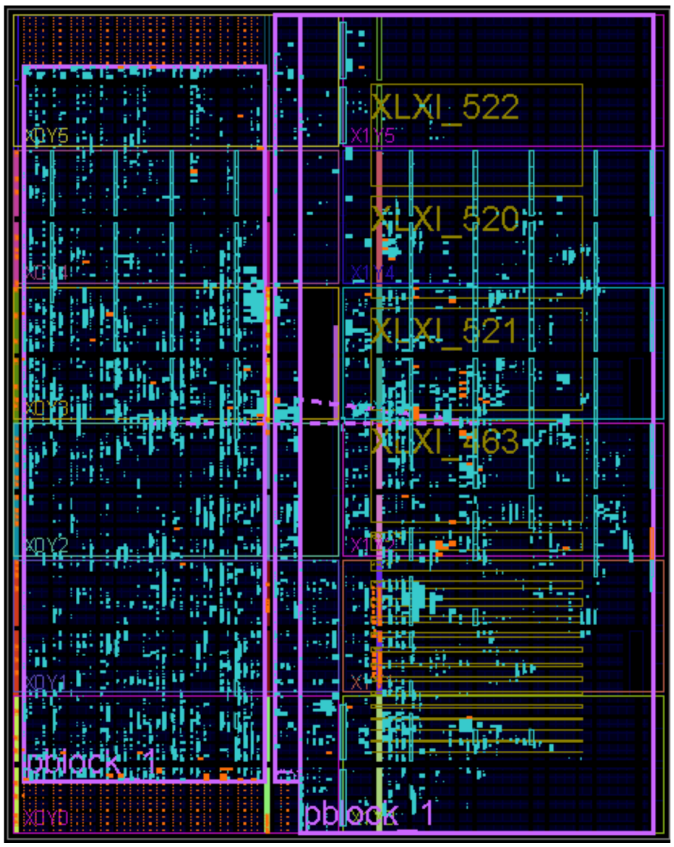

Figure 4. Placement and area constraints in the ISE Design Suite.

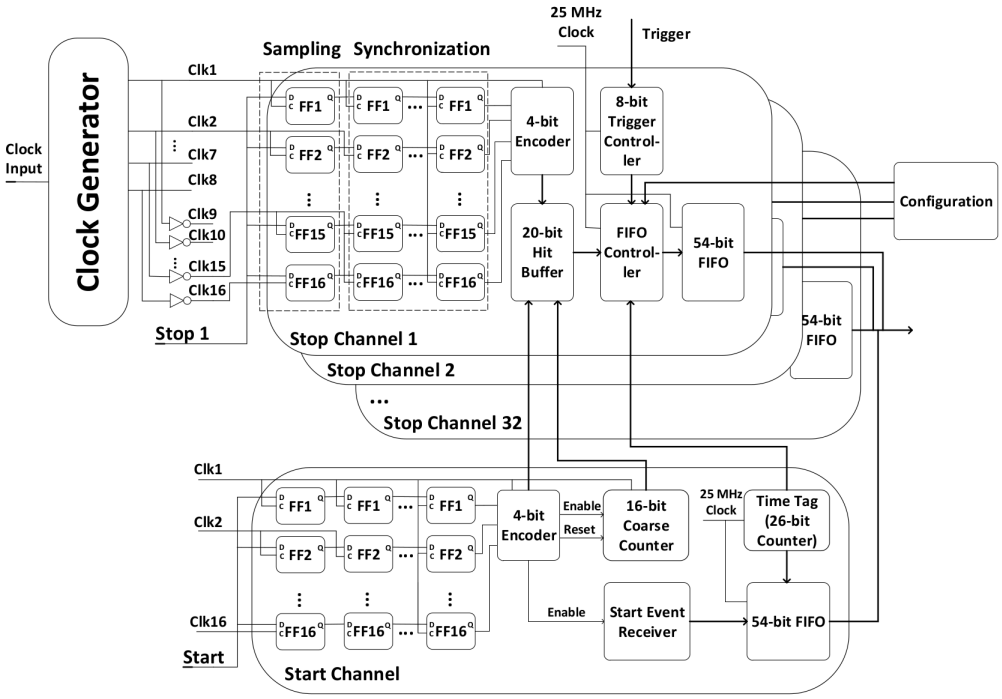

Figure 5. Schematic of the 32-channel TDC structure.

hit buffer as the final measurement for the time difference between start and stop. The hit buffer storage value was set to 512, so the hit buffer can continuously receive 512 valid events until the next start signal arrives; it can also be increased or decreased if necessary. Because the coarse counter is a 16-bit counter driven by a 200-MHz clock, the measuring duration can extend to 327.68 μs. Considering that it may be used in conjunction with an external trigger system in the future, an 8-bit trigger controller is used to receive the external trigger signal. It is a delay-adjustable controller that analyses the event and the external trigger signal to determine if the event is valid, and to record the number of triggers. A 26-bit counter driven by a 25-MHz clock is used as a time tag to record the arrival time of each event. Its allowable measurement duration exceeds the interval of the two pulsed muon beams (2.5 Hz repetition rate). This tag is purposed to provide a global time reference that can be used to construct the data set. The First Input First Output (FIFO) controller stores a 20-bit hit count, an 8-bit trigger count, and a 26-bit time tag into the 54-bit FIFO. It is also responsible for receiving and processing configuration commands from the Gigabit Ethernet, including time window settings and channel shielding. The start event is received by the start event receiver and written to a 54-bit FIFO with the time tag.

1.3 Gigabit Ethernet transmission

The low count rate of a single channel means that the μSR experiments are likely to have more channels. J-PARC developed a new 1280-channel μSR spectrometer in 2014 [12]. We use FPGA-based Gigabit Ethernet to achieve high-speed data transmission, as this enables application to thousands, or even tens of thousands, of channels. The schematic of Gigabit Ethernet transmission is as shown in figure 6. The data transfer clock operates at 125 MHz, using eight bits of data.

2019 JINST 14 T06002

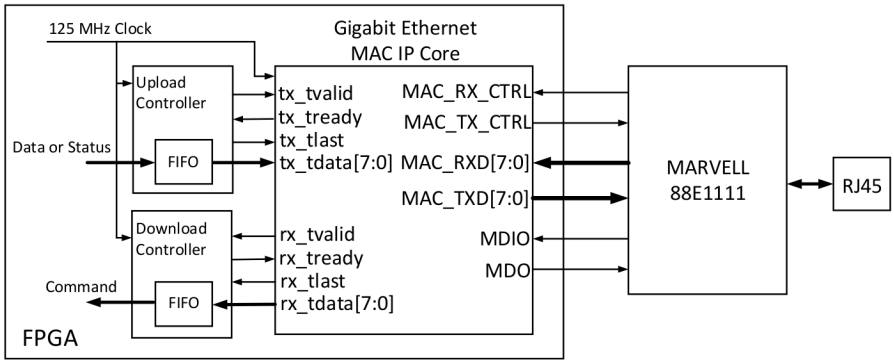

Figure 6. Schematic of the Gigabit Ethernet transmission.

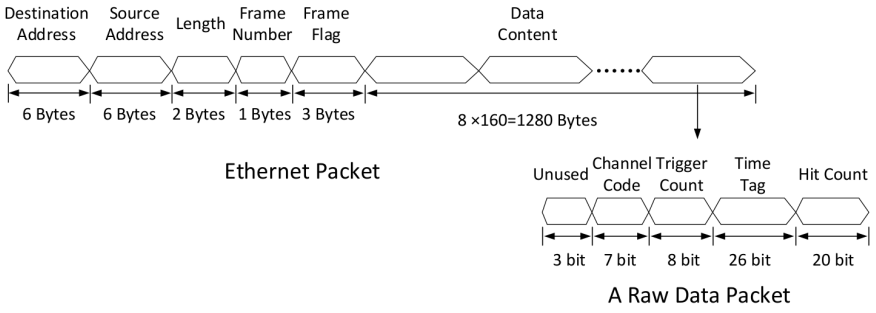

Figure 7. Data format of an Ethernet packet and a raw data packet.

Within the FPGA, the Xilinx Gigabit Ethernet IP core operates in the media access control layer. A Gigabit Ethernet transceiver (88E1111 produced by Marvell), which is a physical layer device. The data or status information is uploaded to the host computer via the upload controller. The command issued by the host computer is downloaded to the FPGA via the download controller.

This Gigabit Ethernet is based on a custom transport protocol. Every time the host computer sends a data upload command, 256 frames of an Ethernet packet are uploaded. An Ethernet packet has 1298 bytes, as shown in figure 7. It includes a 6-byte destination address, a 6-byte source address, a 2-byte length flag, a 1-byte frame number, a 3-byte frame flag, and 1280-byte data content. The frame flag is used to distinguish whether the packet is a data packet, status packet or command packet. A data packet contains 160 raw data packets, each of which consists of three unused bits, a 7-bit channel code, an 8-bit trigger count, a 26-bit time tag and a 20-bit hit count. The unused three bits can be used to extend the channel code. The current spectrometer prototype has 128 channels, and one TDC module has 32 channels. Therefore, seven bits are used for channel coding, and four different Media Access Control (MAC) addresses are written into the logic. The unique MAC address and corresponding 32 channel codes are determined by the hardware jumpers. More MAC addresses can be written into the logic, and the length of the channel code can be extended to enable simultaneous operation of more TDC modules.

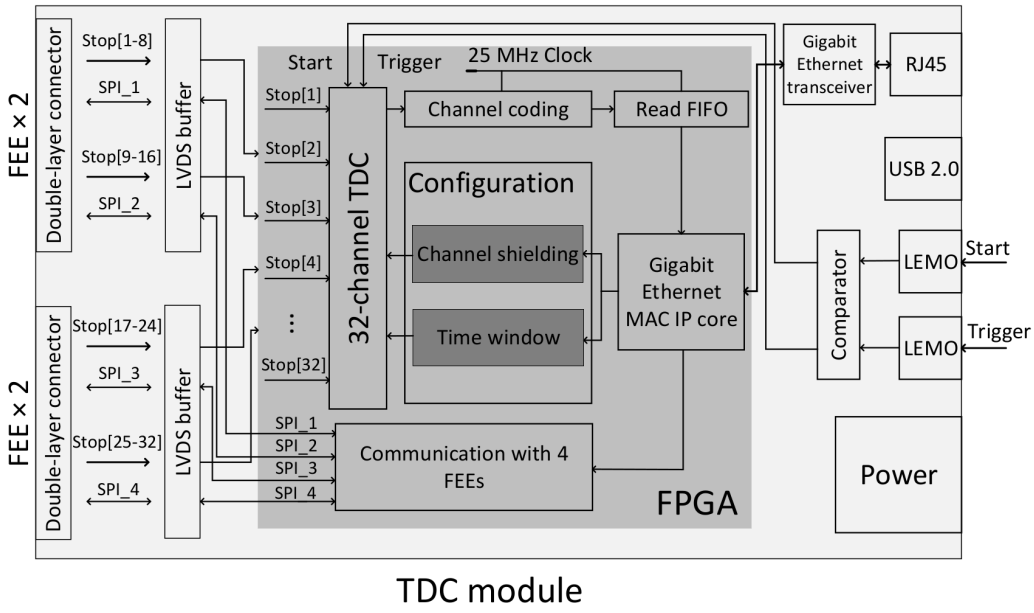

Figure 8. Schematic of the TDC module.

1.4 TDC module implementation

A schematic of the TDC module is shown in figure 8. The 54-bit FIFO data for each TDC channel is detected every clock cycle; then, the data is written to the 64-bit read FIFO according to a certain priority (start channel > stop channel 1 > . . . > stop channel 32) after 7-bit channel coding. Multiple raw data packets are packaged into an Ethernet packet by the upload controller for uploading to the data acquisition (DAQ) software. Because each raw packet is 64 bits, a 25-MHz clock does not limit the data upload speed via the Gigabit Ethernet. The time window settings (including high and low thresholds) allow the user to filter the events within a certain time window. Users can also implement channel shielding to manually close certain channels that are exhibiting undesired behaviour for reasons such as a broken detector. The 8-channel FEE is used to convert the signals of PMT detectors into timing pulses with a timing precision of 55 ps [14]. For time measurement, the four FEEs are connected to one TDC module via two 68-pin double-layer connectors. The TDC module communicates with each FEE via a serial peripheral interface to control the discrimination threshold. The start and trigger signals are connected to the FPGA by two LEMO connectors. The TDC module, which has a standard NIM module design, is shown in figure 9.

2 Test results and discussion

2.1 DNL, INL and resolution

The code density method was used to test the bin widths of each TDC channel. An Agilent 81180A dual-channel arbitrary waveform generator was used to generate two periodic pulse signals. The signal frequency for the start channel is controlled to correlate with the sampling clock frequency. Conversely, the signal frequency for the stop channel is controlled to non-correlate with the sampling clock frequency. The data packets are uploaded to the computer via the Gigabit Ethernet. The

2019 JINST 14 T06002

Figure 9. NIM TDC module.

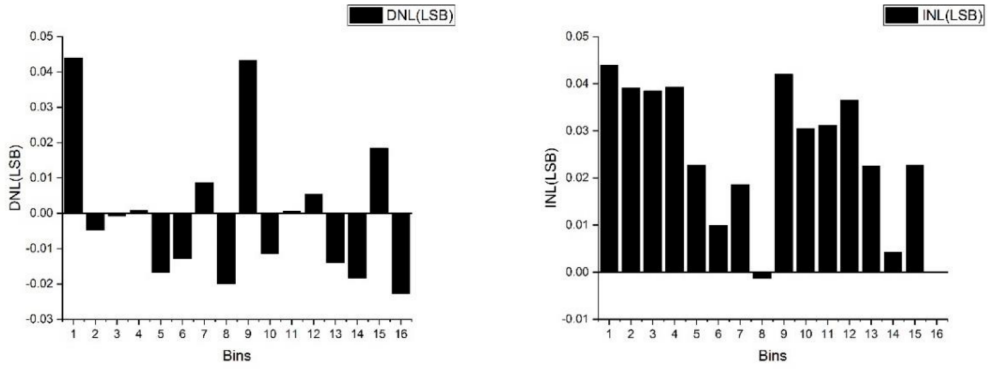

Figure 10. DNL of one TDC channel as measured via the code density method. (b). INL of one TDC channel as measured via the code density method.

hit signals of the start channel are at a fixed position within the sampling clock cycle, and the hit signals of the stop channel have an equal probability at all position. Therefore, the probability of hit signals detected in each TDC bin reflects the TDC bin width. Figure 10 shows typical differential nonlinearity (DNL) and integral nonlinearity (INL) measurements for one TDC channel. As can be seen, the measured DNL and INL are each less than 0.044 Least Significant Bit (LSB). Because the maximum routing skew is only 4 ps / 312.5 ps = 0.013 LSB, the DNL and INL are primarily determined by the skew of the sampling clocks. The clk(N+8) is the inversion of the clkN, as shown in figure 5; thus, we can see from figure 10(a) that the DNL of the Nth bin is not significantly different from the DNL of the (N+8) bin, where N ranges from 1 to 8.

The RMS time resolution was measured by operating the Agilent 81180A dual-channel arbitrary waveform generator such that it produces two periodic pulse signals of the same frequency that are not correlated with the sampling clock. The two pulse signals were respectively transmitted to the start and stop channels, and the time interval was randomly set. The test results are shown in figure 11. The dual-channel RMS resolution was less than 184.7 ps.

2019 JINST 14 T06002

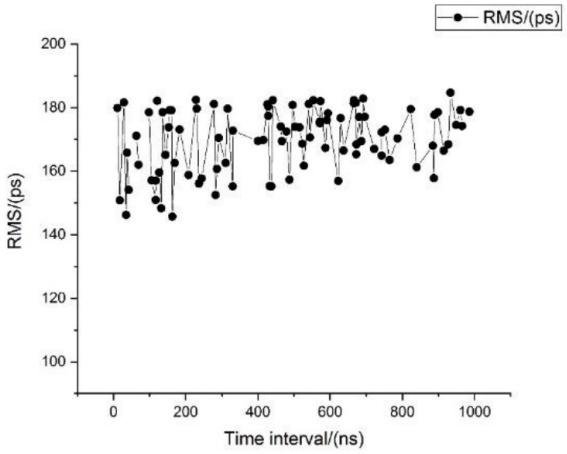

Figure 11. Dual-channel (start and stop channels) RMS time resolution.

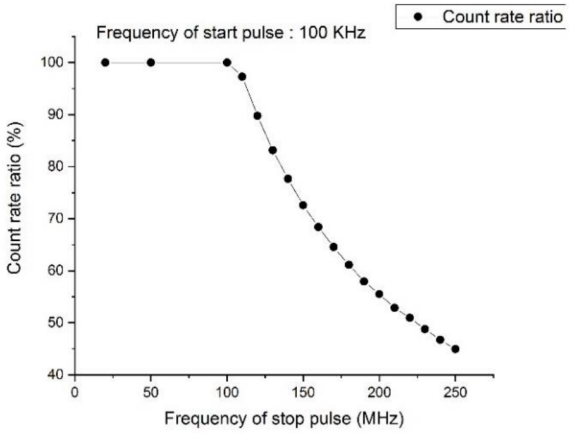

Figure 12. Count rate ratio for different stop pulse frequencies.

2.2 Dead time

In order to test the dead time of the TDC, Channel 1 of the Agilent 81180A dual-channel arbitrary waveform generator was configured to trigger mode, in which the trigger interval and number of triggers were respectively set to 10 ms (corresponding to a 100-kHz frequency) and eight; additionally, the SYNC output was set to generate a single pulse signal that is synchronized with Channel 1, the output of which was connected to a stop channel; the SYNC output was connected to the start channel. Therefore, with this configuration, one start signal is linked to eight consecutive stop signals. The pulse signal frequency of Channel 1 was gradually increased from 20 to 250 MHz. The obtained data were then separately analysed. The ratio of the actual count rates to the theoretical count rates is shown in figure 12 for various frequencies. As shown, the count rate ratio was close to 100% when the stop pulse frequency was less than 100 MHz. Figure 13 shows the statistical results for the counts as a function of the time interval when the stop pulse frequency was 100 MHz. The counts of each group were equal (i.e., equal to the counts of the start channel). Thus, the dead time of the TDC is less than 1/100 MHz = 10 ns.

2019 JINST 14 T06002

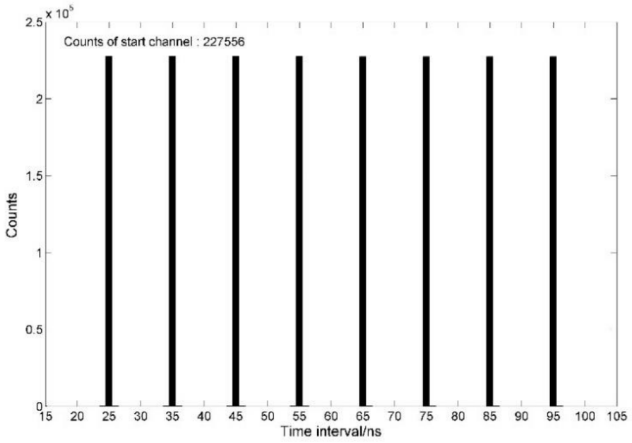

Figure 13. Counts as a function of the time interval under the condition of a stop pulse frequency of 100 MHz.

2.3 Discussion

The effects of the Agilent 81180A dual-channel arbitrary waveform generator were taken into account in the determination of the RMS time resolution of the tested TDC. However, its resolution was 10 ps, which is negligible.

Note that the maximum transmission rate of the Gigabit Ethernet is limited by various factors specific to the computer, such as the central processing unit (CPU) computing speed, hard disk access speed, operating system and type of Ethernet cable. The test described here is relatively simple. A 64-bit counter was used as the data source of the FPGA. We used an ordinary computer (Window 7 operating system, i5-2320 CPU, Network adapter: Realtek PCIe GBE Family Controller) to receive the data. The test results show that all data were continuous. The clock frequency of the counter can be increased to make the Gigabit Ethernet operate at full load, and the data can be discarded after being received. A total of 30.5 GB (3.2×10^{10} bytes) of data was uploaded in 312 s; thus, the maximum transmission rate of the Gigabit Ethernet is 840.2 Mbps.

The count rate of the μSR experiments was very low. The current spectrometer prototype has 128 channels; therefore, the total transmission rate is 110 counts/pulse × 2.5 pulse/s × 64 bit/count × 128 = 2.3 Mbps. Even if the number of channels is increased to 10,000 in the future, the total transmission rate will only be 176 Mbps, which does not significantly affect the speed of the Gigabit Ethernet.

3 Conclusion

A 32-channel NIM TDC electronic readout unit module was specifically designed for the CSNS μSR spectrometer prototype. 32 TDC channels, Gigabit Ethernet data transmission and communication with four 8-channel FEEs are implemented in a single Xilinx Virtex-6 FPGA. One start channel and 32 stop channels are included. By incorporating LUTs and placement and area constraints, the routing skew of all channels was reduced to less than 4 ps; consequently, the routing skew is no longer a factor that limits the resolution of the multi-phase clock sampling-based TDC. The duration between the start event and each stop event is directly measured, and the arrival time of

2019 JINST 14 T06002

each event is recorded. Each TDC channel has a hit storage value of 512, the measurement duration can range from 0 to 327.68 μs. The RMS time resolution and dead time are less than 184.7 ps and 10 ns, respectively. Additionally, FPGA-based Gigabit Ethernet data transmission is implemented for high-speed data uploads. Users can use the Gigabit Ethernet to set a time window and shield certain channels for the TDC. The results of testing show that the overall performance satisfies the desired requirements for μSR experiments. To realize the application of China's μSR spectrometer prototype, the entire DAQ system, including 16 FEEs, 4 TDC module and DAQ software, is currently being tested, and satisfactory results are expected in the near future. In addition, a SiPM array-based 128-channel TDC module is being designed for the next generation of μSR spectrometer. Owing to the enhanced integration of SiPM arrays, more channels have to be added to the TDC module in a way that does not degrade the performance.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (NSFC) (grant number 11527811). Additionally, the authors would like to thank Xiaojie Ni and Ziwen Pan for their support during the testing process.

References

[1] A. Schenck, *Muon spin rotation spectroscopy: principles and applications in solid state physics*, Bristol, Boston U.S.A. (1985).

[2] A. Yaouanc and P. Dalmas de Réotier, *Muon spin rotation, relaxation and resonance: applications to condensed matter*, Oxford University Press, Oxford U.K. (2011).

[3] *ISIS neutron and muon source*, https://www.isis.stfc.ac.uk/Pages/Muons.aspx.

[4] *Japan Proton Accelerator Research Complex*, http://www.j-parc.jp/MatLife/en/index.html.

[5] *The Paul Scherrer institute*, https://www.psi.ch/lmu/.

[6] *TRIUMF*, http://cmms.triumf.ca/ (2018).

[7] J.Y. Tang, S.N. Fu and J. Wei, *Characteristics and potential applications of the proton beams at the CSNS*, *J. Korean Phys. Soc.* **52** (2008) 710.

[8] H.T. Jing et al., *Production target and muon collection studies for an experimental muon source at CSNS*, *Nucl. Instrum. Meth.* **A 684** (2012) 109.

[9] R. Xiao et al., *A new muon-pion collection and transport system design using superconducting solenoids based on CSNS*, *Chin. Phys.* **C 40** (2016) 99.

[10] J.Y. Tang et al., *EMuS muon facility and its application in the study of magnetism*, *Quant. Beam Sci.* **2** (2018) 23.

[11] S.Y. Suzuki et al., *New pipelined data acquisition system for μSR experiments at J-PARC*, *Nucl. Instrum. Meth.* **A 600** (2009) 53.

[12] K.M. Kojima et al., *New μSR spectrometer at J-PARC MUSE based on Kalliope detectors*, *J. Phys. Conf. Ser.* **551** (2014) 012063.

[13] Y.G. Wang, P. Kuang and C. Liu, *A 256-channel multi-phase clock sampling-based time-to-digital converter implemented in a Kintex-7 FPGA*, *IEEE Int. Instrum. Meas. Technol. Conf. Proc.* (2016).

[14] M.Q. Zhuang et al., *The design of front-end electronics prototype for μSR spectrometer*, *Nucl. Electron. Detect. Technol.* **37** (2017).

2019 JINST 14 T06002