Des. Codes Cryptogr. (2015) 77:479–491
DOI 10.1007/s10623-015-0084-4

Optimal low-power coding for error correction and crosstalk avoidance in on-chip data buses

Yeow Meng Chee[1] · Charles J. Colbourn[2] · Alan Chi Hung Ling[3] · Hui Zhang[1] · Xiande Zhang[1]

Received: 30 October 2014 / Revised: 12 April 2015 / Accepted: 16 April 2015 /
Published online: 8 May 2015

Abstract Coupled switched capacitance causes crosstalk in ultra deep submicron/nanometer VLSI fabrication, which leads to power dissipation, delay faults, and logical malfunctions. We present the first memoryless transition bus-encoding technique for power minimization, error-correction, and elimination of crosstalk simultaneously. To accomplish this, we generalize balanced sampling plans avoiding adjacent units, which are widely used in the statistical design of experiments. Optimal or asymptotically optimal constant weight codes eliminating each kind of crosstalk are constructed.

Keywords Constant weight codes · Packing sampling plan avoiding adjacent units · Crosstalk avoidance · Low power code · Packing by triples · Balanced sampling plan

Mathematics Subject Classification 94B25 · 05B40 · 05B07 · 62K10

This is one of several papers published in *Designs, Codes and Cryptography* comprising the "Special Issue on Cryptography, Codes, Designs and Finite Fields: In Memory of Scott A. Vanstone".

✉ Charles J. Colbourn
charles.colbourn@asu.edu

Yeow Meng Chee
ymchee@ntu.edu.sg

Alan Chi Hung Ling
aling@emba.uvm.edu

Hui Zhang
huizhang@ntu.edu.sg

Xiande Zhang
xiandezhang@ntu.edu.sg

1 Division of Mathematical Sciences, School of Physical and Mathematical Sciences, Nanyang Technological University, Singapore 637371, Singapore

2 School of Computing, Informatics, and Decision Systems Engineering, Arizona State University, Tempe, AZ 85287, USA

3 Department of Computer Science, University of Vermont, Burlington, VT 05405, USA

1 Introduction

The ever-decreasing feature size of VLSI fabrication process has led to many challenges in VLSI circuit design. One of the most important issues concerns the characteristics of on-chip wires [11]. The wires' cross-sectional areas and spacings have fallen dramatically with the move into the ultra deep submicron/nanometer (UDSM) regime. This has increased the resistance and capacitance of wires. To help reduce resistance, wires today are taller than they are wide, and they are poised to grow even taller as technology continues to scale. The resulting growth of side-to-side capacitance between long parallel wires causes coupled switch capacitance to dominate the wire-to-substrate capacitance in UDSM circuits by several orders of magnitude [21]. Coupled switched capacitance in turn leads to *crosstalks*, which result in power dissipation, delay faults, and logical malfunctions. The problem of eliminating or minimising crosstalks is considered the biggest signal integrity challenge for long on-chip buses implemented in UDSM CMOS technology [12].

The worst crosstalk couplings have been classified into four types [6,12], as described in Table 1. The coupled switched capacitance resulting from type-1, -2, -3, and -4 crosstalks is in the ratio of 1:2:3:4. Hence, it is particularly important to avoid crosstalks of higher types. Type-1 crosstalks cannot be avoided in any useful communication channel. However, type-1 crosstalks give rise to power dissipation and must be limited, because low power is a critical design objective in recent years.

Another factor that has emerged as a new challenge for VLSI circuit designers is UDSM noise, caused by high-leakage transistors, power-grid fluctuations, ground bounce, IR drops, clock jitter, and electromagnetic radiation. The effects of such noise are difficult to predict or prevent. For example, noise in radiation-hardened circuits for satellite communication systems is random and does not correlate with particular switching patterns on the buses. A further source of faults is manufacturing defects. In nanotechnology, circuits are manufactured with a significant proportion of faults, and occasional errors may be unavoidable. Hence, preventive techniques are insufficient, and active error correction is required.

Various researchers have proposed coding techniques to encode data on a bus for crosstalk avoidance [6,17,28], for low power dissipation [3,15,19,22,26], and for error correction [1,8]. Coding schemes that simultaneously satisfy two of these three criteria have also been investigated:

- crosstalk avoidance and low power dissipation [12,27];
- crosstalk avoidance and error correction [14]; and
- low power dissipation and error correction [2,16,18].

Table 1 Types of worst crosstalk couplings

Type-1	Type-2	Type-3	Type-4
$0 \longleftrightarrow 1$	$001 \longleftrightarrow 110$ $011 \longleftrightarrow 100$	$001 \longleftrightarrow 010$ $010 \longleftrightarrow 100$ $011 \longleftrightarrow 101$ $101 \longleftrightarrow 110$	$010 \longleftrightarrow 101$
Single wire undergoes transition. Adjacent wires maintain previous states	Center wire in opposite transition to an adjacent wire. The other wire in same transition as center wire	Center wire in opposite transition to an adjacent wire. The other wire maintains previous state	All three adjacent wires undergo opposite transitions

Despite many efforts, the only families of optimal codes known are those for low power dissipation [3]. Many of the results on the comparative performance of existing codes are based on simulations rather than rigorous mathematical analysis.

In this paper, we begin the study of codes for UDSM buses that simultaneously provide for low power dissipation, crosstalk avoidance, and error correction. In particular, we exhibit the first infinite families of such codes that are provably optimal.

The paper is organized as follows. Section 2 establishes necessary terminology and gives a mathematical formulation of the problem of designing low-power codes that avoid crosstalks and correct errors. In Sect. 3, we present the relation of codes of each type with packing sampling plans avoiding adjacent units. In Sect. 4, we focus on optimal solutions for $k = 3$ for all positive integer n. In Sect. 5, the sizes of optimal codes of all types with small lengths are determined by computer search, and brief conclusion is given.

2 Background

2.1 Coding framework

A coding framework for data buses was introduced by Ramprasad et al. [15]. A bus interconnecting two embedded systems on a *systems-on-chip* (SoC) platform can be modelled generically as in Fig. 1. The *source encoder* (*decoder*) compresses (decompresses) the input data so that the number of bits required in the representation of the source is minimised. While the source encoder removes redundancy, the *channel encoder* adds redundancy to combat errors that may arise due to noise in the bus.

Ramprasad et al. [15] considered various combinations of source-channel encoder-decoder pairs and presented simulation results for their power dissipation. Their approach is what is known as *joint source-channel coding* in the information theory literature. *Shannon's information separation theorem* [20] states that reliable transmission can be accomplished by separate source and channel coding, where the source encoder and decoder need not take into account the channel statistics and the channel encoder and decoder need not take into account the source statistics. This applies, however, only for point-to-point transmissions and for infinite sequence length. The first condition (point-to-point transmission) holds for a UDSM bus but the second requirement for infinite sequence length is clearly undesirable for bus coding, because it could give rise to circuits of unbounded delay. Moreover, joint source-channel coding is useful only when we know the statistics of the source and channel. In the absence of such statistics, one can only fall back on optimising the source and channel separately. Indeed, Ramprasad et al. [15] considered coding schemes and simulations on certain source data with better understood statistics (for example, pop music, classical music, video, and speech).

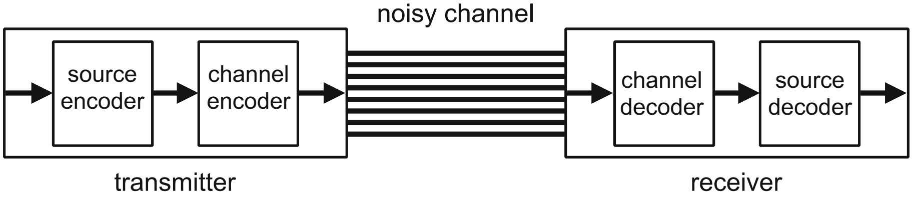

Fig. 1 Framework for systems-on-chip

In many systems, the behaviour of source data is hard to predict and so the joint source-channel coding approach loses its power. Many researchers have therefore fallen back on addressing the source coding and channel coding problems separately. This is also the approach taken in this paper. We focus on designing optimal channel coding schemes for the scenario where the source statistics are unknown.

2.2 Codes

The *Hamming n-space* is the set $\mathcal{H}(n) = \{0, 1\}^n$, endowed with the (*Hamming*) *distance* $d_H(\cdot, \cdot)$ defined as follows: for $\mathsf{u}, \mathsf{v} \in \mathcal{H}(n)$, $d_H(\mathsf{u}, \mathsf{v})$ is the number of positions where u and v differ. The (*Hamming*) *weight* of a vector $\mathsf{u} \in \mathcal{H}(n)$ is the number of positions in u with nonzero value, and is denoted $w_H(\mathsf{u})$. The ith component of u is denoted u_i. The *support* of a vector $\mathsf{u} \in \mathcal{H}(n)$, denoted $\text{supp}(\mathsf{u})$, is the set $\{i : \mathsf{u}_i = 1\}$.

A (*binary*) *code of length n* is a subset $\mathcal{C} \subseteq \mathcal{H}(n)$. $\mathcal{C}$ is said to be of *constant weight w* if $w_H(\mathsf{u}) = w$ for all $\mathsf{u} \in \mathcal{C}$. The elements of a code are called *codewords* and the *size* of a code is the number of codewords it contains. The *support* of $\mathcal{C}$ is $\text{supp}(\mathcal{C}) = \{\text{supp}(\mathsf{u}) : \mathsf{u} \in \mathcal{C}\}$. The *minimum distance* of $\mathcal{C}$ is $d_{\min}(\mathcal{C}) = \min\{d_H(\mathsf{u}, \mathsf{v}) : \mathsf{u}, \mathsf{v} \in \mathcal{C} \text{ and } \mathsf{u} \neq \mathsf{v}\}$. A constant-weight code of length n, minimum distance d, and weight w is denoted as an (n, d, w) code.

A code that is capable of correcting any occurrence of e or fewer symbol errors is said to be *e-error-correcting*. A code $\mathcal{C}$ is e-error-correcting if and only if $d_{\min}(\mathcal{C}) \geq 2e + 1$ [9].

2.3 Set systems and graphs

For integers $i < j$, the set $\{i, i + 1, \ldots, j\}$ is abbreviated as $[i, j]$. We further abbreviate $[1, j]$ to $[j]$. For a finite set X and $k \leq |X|$, we define

$$2^X = \{B : B \subseteq X\}, \quad \text{and} \quad \binom{X}{k} = \{B \subseteq X : |B| = k\}.$$

A *set system* is a pair $\mathcal{S} = (X, \mathcal{B})$, where X is a finite set of *points* and $\mathcal{B} \subseteq 2^X$. The elements of $\mathcal{B}$ are called *blocks*. The *order* of $\mathcal{S}$ is the number of points, $|X|$, and the *size* of $\mathcal{S}$ is the number of blocks, $|\mathcal{B}|$. A set system $(X, \mathcal{B})$ is said to be *k-uniform* if $\mathcal{B} \subseteq \binom{X}{k}$. A *graph* is a 2-uniform set system and it is common to refer to the points and blocks of a graph as vertices and edges, respectively. A *path* of length n is an alternating sequence of vertices and edges $W = v_0, e_1, v_1, e_2, \ldots, e_n, v_n$, such that all the vertices v_i, $i \in [0, n]$ and edges $e_i, i \in [n]$ are all distinct from one another, except possibly the first and last vertices. A *cycle* is a path in which the first and last vertices are the same.

Let $(X, \mathcal{B})$ be a set system of order n. The *incidence vector* of a block $B \in \mathcal{B}$ is the vector $\iota(B) \in \mathcal{H}(n)$ such that

$$\iota(B)_i = \begin{cases} 1, & \text{if } i \in B \\ 0, & \text{otherwise.} \end{cases}$$

There is a natural correspondence between the Hamming n-space and the *complete* set system $(X, 2^X)$: the positions of vectors in $\mathcal{H}(n)$ correspond to points in X, a vector $\mathsf{u} \in \mathcal{H}(n)$ corresponds to the block $\text{supp}(\mathsf{u})$, and $d_H(\mathsf{u}, \mathsf{v}) = |(\text{supp}(\mathsf{u}) \setminus \text{supp}(\mathsf{v})) \cup (\text{supp}(\mathsf{v}) \setminus \text{supp}(\mathsf{u}))|$. From this, it follows that there is a bijection between the set of all codes of length n and the set of all set systems of order n.

An (n, k, λ)-packing is a k-uniform set system $(X, \mathcal{B})$ with $|X| = n$ such that every element of $\binom{X}{2}$ is contained in at most λ blocks of $\mathcal{B}$. Let $D(n, k, \lambda)$ denote the largest size among all (n, k, λ)-packings. The *leave graph* of $(X, \mathcal{B})$ is the multigraph (X, E), where E

contains each $e \in \binom{X}{2}$ exactly $\lambda - d(e)$ times, where $d(e)$ is the number of blocks containing e. When $\lambda = 1$, we omit λ in the notation; in this case, the leave is a simple graph. When the leave contains no edges, the packing is a *balanced incomplete block design*.

The *balanced sampling plan avoiding adjacent units* (BSA) was introduced to design sampling plans that exclude contiguous units in statistical experiments [10,25]; for more recent work, see [7,29]. In statistical applications, in a circular or linear order of the elements, elements that are "close" do not appear together, while those more distant all appear the same number of times together. A (*circular*) $BSA_\lambda(n, k; \alpha)$ is an (n, k, λ)-packing $(X, \mathcal{B})$ with $X = \mathbb{Z}_n$ whose leave graph consists of all the edges $\{i, j\}$ with $i - j \equiv \pm 1, \ldots, \pm\alpha \pmod n$, and every other pair appears in λ blocks. A (*linear*) $LBSA_\lambda(n, k; \alpha)$ is an (n, k, λ)-packing $(X, \mathcal{B})$ with $X = [0, n-1]$ whose leave graph consists of all the edges $\{i, j\}$ with $0 \le i < j < n$ for which $j - i \le \alpha$, and every other pair appears in λ blocks. We employ these only when $\lambda = 1$, and so omit λ in the notation.

We generalize circular and linear BSAs (with $\lambda = 1$) to a *packing sampling plan avoiding adjacent units* (PSA). A (*circular*) CPSA$(n, k; \alpha)$ is an (n, k)-packing $(X, \mathcal{B})$ with $X = \mathbb{Z}_n$ whose leave graph contains all the edges $\{i, j\}$ with $i - j \equiv \pm 1, \ldots, \pm\alpha \pmod n$, and every other pair appears in *at most one* block. A (*linear*) LPSA$(n, k; \alpha)$ is an (n, k)-packing $(X, \mathcal{B})$ with $X = [0, n-1]$ whose leave graph contains all the edges $\{i, j\}$ with $0 \le i < j < n$ for which $j - i \le \alpha$, and every other pair appears in *at most one* block. (In this case, every CPSA$(n, k; \alpha)$ is an LPSA$(n, k; \alpha)$ but the converse need not hold.) Let $B(n, k; \alpha)$ denote the largest size of any LPSA$(n, k; \alpha)$; the LPSA is *optimal* if its size is $B(n, k; \alpha)$. Similarly, let $B^\circ(n, k; \alpha)$ denote the largest size of any CPSA$(n, k; \alpha)$; the CPSA is *optimal* if its size is $B^\circ(n, k; \alpha)$.

Let $U(n, k; \alpha) = \left\lfloor \frac{2\sum_{i=0}^{\alpha-1}\left\lfloor \frac{n-\alpha-i-1}{k-1}\right\rfloor + (n-2\alpha)\left\lfloor \frac{n-2\alpha-1}{k-1}\right\rfloor}{k} \right\rfloor$.

Lemma 2.1 $B(n, k; \alpha) \le U(n, k; \alpha)$.

Proof For an LPSA$(n, k; \alpha)$ constructed on $[0, n-1]$, for each $i \in [0, \alpha - 1]$, the points i and $n - 1 - i$ appear in at most $\left\lfloor \frac{n-\alpha-i-1}{k-1} \right\rfloor$ blocks, and all the other points appear in at most $\left\lfloor \frac{n-2\alpha-1}{k-1} \right\rfloor$ blocks. Then $kB(n, k; \alpha) \le 2\sum_{i=0}^{\alpha-1}\left\lfloor \frac{n-\alpha-i-1}{k-1}\right\rfloor + (n-2\alpha)\left\lfloor \frac{n-2\alpha-1}{k-1}\right\rfloor$. $\square$

When $\alpha = 1$, we omit it in the notation. If there is an (n, k)-packing with leave graph containing a path of length $n - 1$, we can always relabel the points to get an LPSA(n, k).

Corollary 2.2 $B(n, k) \le \left\lfloor \frac{2\left\lfloor \frac{n-2}{k-1}\right\rfloor + (n-2)\left\lfloor \frac{n-3}{k-1}\right\rfloor}{k} \right\rfloor$.

Theorem 4.1 shows that when $k = 3$, this inequality is tight.

2.4 Problem formulation

Limited weight codes have been widely exploited for the case of on-chip communication to achieve crosstalk coupling elimination and energy efficiency [12,23]. We consider an n-bit parallel bus in a single metal layer, for which we want memoryless codes to weaken crosstalk, reduce power consumption, and correct errors. We use constant weight codes with small weight to achieve low power similarly by reducing the node switching activity, that is, reducing the total number of transitions occurring between the newly arrived data and the present data on the bus.

Assume an n-bit bus, consisting of signals $b_0, b_1, b_2, \ldots, b_{n-1}$. Consider a group of three wires in an on-chip bus, which are driven by signals b_{i-1}, b_i and b_{i+1}. The delay and energy consumption are primarily affected by transition patterns based on the bus signals b_{i-1}, b_i and b_{i+1} as the crosstalk patterns in Table 1.

The selection of codeword does not depend on previous history, so the environment is *memoryless*. Consequently coding must address the possibility that any two codewords can appear one after the other. Therefore to avoid crosstalk and correct errors, we are interested in constant weight codes of length n, weight w and minimum distance $d \geq 3$ satisfying the condition that there do not exist three consecutive coordinates $i-1, i, i+1$ such that the crosstalk couplings of type-2 (or -3, -4) occur in any two different codewords.

We denote such a code avoiding crosstalk of each type as an (n, d, w)-II (or -III, -IV) code. The maximum size of these codes are denoted as $A^{II}(n, d, w)$ (or $A^{III}(n, d, w)$, $A^{IV}(n, d, w)$), and any code achieving this size is *optimal*. When $\mathcal{S} \subseteq \{II, III, IV\}$, the maximum size of a code that is simultaneously an (n, d, w)-S code for each $S \in \mathcal{S}$ is denoted by $A^{\mathcal{S}}(n, d, w)$.

When $d = 2w$, the following results are straightforward.

Lemma 2.3 *For all positive integers n and w,*

(i) $A^{II}(n, 2w, w) = A^{IV}(n, 2w, w) = \left\lfloor \frac{n}{w} \right\rfloor$;
(ii) $A^{III}(n, 2w, w) = \left\lfloor \frac{n}{w} \right\rfloor$ *when* $w \neq 1$; $A^{III}(n, 2, 1) = \left\lfloor \frac{n+1}{2} \right\rfloor$.

Proof The quantity $s = \left\lfloor \frac{n}{w} \right\rfloor$ is an upper bound on the size of the desired code in each case. We construct codes of size s as follows. The code with support

$$\{\{i, s+i, 2s+i, \ldots, (w-1)s+i\} : i \in [0, s-1]\}$$

is an optimal $(n, 2w, w)$-II code. The code with support

$$\{\{wi, 1+wi, \ldots, (w-1)+wi\} : i \in [0, s-1]\}$$

is an optimal $(n, 2w, w)$-IV code, and an optimal $(n, 2w, w)$-III code when $w \neq 1$. When $w = 1$, the code with support $\{\{2i\} : i \in [0, \left\lfloor \frac{n-1}{2} \right\rfloor]\}$ is an optimal $(n, 2, 1)$-III code. □

Next we show there is close connection between $(n, 2k-2, k)$ codes of each type and optimal LPSA(n, k)s. Hence, optimal codes are constructed based on the construction of optimal LPSA(n, k)s.

3 Codes and LPSA$(n, k; \alpha)$s

In this section, we establish connections between optimal LPSA$(n, k; \alpha)$s and the codes of each type. We begin with optimal $(n, 2k-2, k)$-II codes for sufficiently large n.

Theorem 3.1 *Let* $k \geq 3$. *Then* $A^{II}(n, 2k-2, k) \geq B(n, k)$. *Further, if* $B(n, k) = U(n, k)$ *and* $n \geq 3k^2 + 2k - 3$, *then* $A^{II}(n, 2k-2, k) = B(n, k)$.

Proof Whenever $(X, \mathcal{B})$ is an LPSA(n, k), the code with support $\mathcal{B}$ is an $(n, 2k-2, k)$-II code. Now suppose that $(X, \mathcal{B})$ is an optimal LPSA(n, k) of size $U(n, k)$. We prove that $U(n, k)$ is the largest possible size of an $(n, 2k-2, k)$-II code. Assume that $\mathcal{D}$ is an $(n, 2k-2, k)$-II code of size M. Partition the code into three parts as follows.

The first part $\mathcal{A}$ contains all codewords with at least one segment "11". Because $n > k$, for each codeword in $\mathcal{A}$, there always exist three adjacent coordinates such that "110" or "011" appears in these coordinates. Let $S = \{i : \exists \mathsf{u} \in \mathcal{A}$, s.t.,$\mathsf{u}$ has "110$''$ in coordinates $i-2, i-1, i$, or "011" in coordinates $i, i+1, i+2\}$, and let $s = |S|$. For each $i \in S$, there exist at most two codewords in $\mathcal{A}$ that have "110" in $i-2, i-1, i$ or "011" in $i, i+1, i+2$. Hence $|\mathcal{A}| \leq 2s$.

The second part $\mathcal{T} \subseteq \mathcal{D} \setminus \mathcal{A}$ contains all codewords with "1" in at least one coordinate in S. Without loss of generality, if there exists a codeword in $\mathcal{A}$ with "110" in the coordinates $i-2, i-1, i$ for some i, then the codewords in $\mathcal{T}$ with "1" in i must have segment "101" in these coordinates to avoid type-2 crosstalk. Because $d_{\min}(\mathcal{D}) = 2k-2$, there is only one such codeword. So for each $i \in S$, there is at most one codeword in $\mathcal{T}$ with "1" in i. Hence $|\mathcal{T}| \leq s$.

Finally, let $\mathcal{C} = \mathcal{D} \setminus (\mathcal{A} \cup \mathcal{T})$. Then $M = |\mathcal{A}| + |\mathcal{T}| + |\mathcal{C}|$. Because each codeword in $\mathcal{C}$ has "0" in all coordinates in S, we can shorten $\mathcal{C}$ to a code $\mathcal{C}'$ by deleting all coordinates in S. Then $\mathcal{C}'$ is an $(n-s, 2k-2, k)$ code, and supp$(\mathcal{C}')$ is an $(n-s, k)$-packing.

The shortening process partitions the coordinates of $\mathcal{C}'$ into at most $s+1$ classes, separated in $\mathcal{C}$ by the coordinates deleted to form $\mathcal{C}'$. No codeword of $\mathcal{C}'$ has "11" in consecutive coordinates of any single class. Let x be the number of isolated coordinates in this partition, and m be the number of classes with at least two coordinates; then $x + m \leq s + 1$. We now estimate the size of $\mathcal{C}'$ using the packing.

Let $a_0 = \left\lfloor \frac{n-s-1}{k-1} \right\rfloor$, $a_1 = \left\lfloor \frac{n-s-2}{k-1} \right\rfloor$, $a_2 = \left\lfloor \frac{n-s-3}{k-1} \right\rfloor$. Then we have:

$$|\mathcal{C}| = |\mathcal{C}'| \leq \left\lfloor \frac{x \cdot a_0 + 2m \cdot a_1 + (n-s-2m-x) \cdot a_2}{k} \right\rfloor.$$

Because $\lfloor x \rfloor - \lfloor y \rfloor - 1 \leq \lfloor x - y \rfloor \leq \lfloor x \rfloor - \lfloor y \rfloor$, we have:

$$\begin{aligned} M &\leq 3s + \left\lfloor \frac{x\left(\left\lfloor \frac{n-s-1}{k-1} \right\rfloor - \left\lfloor \frac{n-s-3}{k-1} \right\rfloor\right) + 2m\left(\left\lfloor \frac{n-s-2}{k-1} \right\rfloor - \left\lfloor \frac{n-s-3}{k-1} \right\rfloor\right) + (n-s)\left\lfloor \frac{n-s-3}{k-1} \right\rfloor}{k} \right\rfloor \\ &\leq 3s + \left\lfloor \frac{x\left(\left\lfloor \frac{2}{k-1} \right\rfloor + 1\right) + 2m\left(\left\lfloor \frac{1}{k-1} \right\rfloor + 1\right) + (n-s)\left\lfloor \frac{n-s-3}{k-1} \right\rfloor}{k} \right\rfloor \\ &\leq 3s + \left\lfloor \frac{2x + 2m + (n-s)\left\lfloor \frac{n-s-3}{k-1} \right\rfloor}{k} \right\rfloor \leq 3s + \left\lfloor \frac{2(s+1) + (n-s)\left\lfloor \frac{n-s-3}{k-1} \right\rfloor}{k} \right\rfloor. \end{aligned}$$

Let $F(s) = 3s + \left\lfloor \frac{2(s+1)+(n-s)\left\lfloor \frac{n-s-3}{k-1} \right\rfloor}{k} \right\rfloor$. We claim that because $n \geq 3k^2 + 2k - 3$, $U(n,k) \geq \max_{s \in [1,n]} F(s)$.

Because $F(s) = 3s + \left\lfloor \frac{2(s+1)+(n-s)\left\lfloor \frac{n-s-3}{k-1} \right\rfloor}{k} \right\rfloor$ and $F(s+1) = 3(s+1) + \left\lfloor \frac{2(s+2)+(n-s-1)\left\lfloor \frac{n-s-4}{k-1} \right\rfloor}{k} \right\rfloor$, we have $\left\lfloor \frac{\left\lfloor \frac{n-s-4}{k-1} \right\rfloor - 2}{k} \right\rfloor - 3 \leq F(s) - F(s+1) \leq \left\lfloor \frac{\left\lfloor \frac{n-s-4}{k-1} \right\rfloor + n-s-2}{k} \right\rfloor - 2$. Further, we have:

$$\left\lfloor \frac{n - 3k^2 - 1 - s}{k(k-1)} \right\rfloor \leq F(s) - F(s+1) \leq \left\lfloor \frac{n-2k-s}{k-1} \right\rfloor.$$

So when $s \leq n - 3k^2 - 1$, $F(s) - F(s+1) \geq 0$, i.e., $F(s)$ is decreasing; and when $s \geq n - 2k$, $F(s) - F(s+1) \leq 0$, i.e., $F(s)$ is increasing. When $s \in [n - 3k^2, n - 2k - 1]$,

$F(s) \leq F(1)$; because the verification is tedious, we omit it here. We therefore only need to compare $F(1)$ and $F(n)$ to find the maximum value of $F(s)$.

$$F(1) - F(n) = 3 + \left\lfloor \frac{4+(n-1)\left\lfloor \frac{n-4}{k-1} \right\rfloor}{k} \right\rfloor - 3n - \left\lfloor \frac{2(n+1)}{k} \right\rfloor \geq \left\lfloor \frac{(n-1)(n-3k^2-1)}{k(k-1)} \right\rfloor.$$

Because $n \geq 3k^2 + 2k - 3 \geq 3k^2 + 1$, $F(1) \geq F(n)$ and $\max_{s\in[1,n]} F(s) = F(1)$.

$$\begin{aligned} U(n,k) - F(1) &\geq \left\lfloor \frac{2\left\lfloor \frac{n-2}{k-1} \right\rfloor + (n-2)\left\lfloor \frac{n-3}{k-1} \right\rfloor - 4 - (n-1)\left\lfloor \frac{n-4}{k-1} \right\rfloor}{k} \right\rfloor - 3 \\ &\geq \left\lfloor \frac{\left\lfloor \frac{n-2}{k-1} \right\rfloor + (n-1)\left\lfloor \frac{n-3}{k-1} \right\rfloor - 4 - (n-1)\left\lfloor \frac{n-4}{k-1} \right\rfloor}{k} \right\rfloor - 3 \\ &\geq \left\lfloor \frac{\left\lfloor \frac{n-2}{k-1} \right\rfloor - 4}{k} \right\rfloor - 3 \geq \left\lfloor \frac{n - 3k^2 - 2k + 3}{k(k-1)} \right\rfloor \geq 0. \end{aligned}$$

Hence $U(n,k) \geq \max_{s\in[1,n]} F(s)$. □

For $(n, 2k-2, k)$-III codes and $(n, 2k-2, k)$-IV codes, we establish lower bounds.

Lemma 3.2 1. $A^{III}(n, 2k-2, k) \geq A^{II,III,IV}(n, 2k-2, k) \geq D(\lceil \frac{n}{2} \rceil, k)$.
2. $A^{III}(n, 4, 3) \geq A^{II,III,IV}(n, 4, 3) \geq B(\lceil \frac{n}{2} \rceil, 3) + \lfloor \frac{n-1}{2} \rfloor$.
3. $A^{III}(n, 4, 3) \geq A^{II,III,IV}(n, 4, 3) \geq B^{\circ}(\lceil \frac{n}{2} \rceil, 3) + \lfloor \frac{n}{2} \rfloor$.

Proof For the first inequality, take an $(\lceil \frac{n}{2} \rceil, k)$-packing $(X, \mathcal{B})$, and construct a code $\mathcal{C}$ of length $\lceil \frac{n}{2} \rceil$ by taking $\operatorname{supp}(\mathcal{C}) = \mathcal{B}$. View $\mathcal{C}$ as an $|\mathcal{B}| \times \lceil \frac{n}{2} \rceil$ array. When $n \equiv 1 \pmod 2$, we add one column of all zeroes between every two consecutive columns of $\mathcal{C}$, and when $n \equiv 0 \pmod 2$ we add one further column of all zeroes after $\mathcal{C}$ to get an $(n, 2k-2, k)$-III code. The verification is straightforward, because every second column is all zeroes.

The construction for the second is similar. Apply the same inflation to an LPSA$\left(\lceil \frac{n}{2} \rceil, 3\right)$ of size $B\left(\lceil \frac{n}{2} \rceil, 3\right)$ to obtain a code $\mathcal{C}_1$. In every codeword of $\mathcal{C}_1$, two 1s are separated by three (or more) coordinates, and different codewords cannot have 1s in adjacent coordinates. Now form code $\mathcal{C}_2$, consisting of all codewords with support $\{2i, 2i+1, 2i+2\}$ for $0 \leq i < \lfloor \frac{n-1}{2} \rfloor$. No prohibited situation arises from 000 or 111 in three consecutive coordinates of a codeword. In consecutive coordinates in which two codewords of $\mathcal{C}_2$ are neither 000 nor 111, the two codewords contain 011 and 110, which is permitted. So we consider one codeword from $\mathcal{C}_1$ and one from $\mathcal{C}_2$. The coordinates with indices in $\{2i + 1 : 0 \leq i < \lfloor \frac{n-1}{2} \rfloor\}$ appear in only one codeword, which is $\{2i, 2i+1, 2i+2\}$. So in the consecutive coordinates in which two such codewords are neither 000 nor 111, and are not equal, the two codewords contain {001, 100}, {010, 011}, or {010, 110}. All are permitted.

The bound in the third case is equal to that in the second unless n is even and $B^{\circ}\left(\lceil \frac{n}{2} \rceil, 3\right) = B\left(\lceil \frac{n}{2} \rceil, 3\right)$. When both occur, use a CPSA to form $\mathcal{C}_1$ and $\mathcal{C}_2$ as in the second case; one further codeword can be added with support $\{0, n-2, n-1\}$. □

Lemma 3.3 $A^{IV}(n, 2k-2, k) \geq B(n, k)$.

Proof Take an LPSA(n, k) $(X, \mathcal{B})$ of size $B(n, k)$. Apply to the points in $[0, n-1]$ the permutation

$$\begin{cases} i \to 2i, \text{ if } i < \lceil n/2 \rceil, \text{ and} \\ i \to 2i - 2\lceil n/2 \rceil + 1, \text{ if } i \geq \lceil n/2 \rceil, \end{cases}$$

to get $(X, \mathcal{B}')$. The code $\mathcal{C}'$ with $\text{supp}(\mathcal{C}') = \mathcal{B}'$ is an $(n, 2k-2, k)$-IV code. □

We give another construction for an $(n, 2k-2, k)$-IV code from an optimal LPSA$(n, k; k-1)$. When $k = 3$, this construction gives a better lower bound than Lemma 3.3.

Lemma 3.4 *Let* $k \geq 3$.

1. $A^{II,IV}(n, 2k-2, k) \geq B(n, k; k-1)$,
2. $A^{IV}(n, 2k-2, k) \geq B(n, k; k-1) + \left\lfloor \frac{n-1}{k-1} \right\rfloor$, *and*
3. $A^{IV}(n, 2k-2, k) \geq B^{\circ}(n, k; k-1) + \left\lfloor \frac{n}{k-1} \right\rfloor$.

Proof Let $s = \left\lfloor \frac{n-1}{k-1} \right\rfloor$, and $(X, \mathcal{B})$ be an LPSA$(n, k; k-1)$ of size $B(n, k; k-1)$. Then the code $\mathcal{C}$ with $\text{supp}(\mathcal{C}) = \{B : B \in \mathcal{B}\}$ is an $(n, 2k-2, k)$-II code and an $(n, 2k-2, k)$-IV code. Further, the code $\mathcal{C}$ with $\text{supp}(\mathcal{C}) = \{B : B \in \mathcal{B}\} \cup \{\{(k-1)i, (k-1)i+1, \ldots, (k-1)i+k-1\} : i \in [0, s-1]\}$ is an $(n, 2k-2, k)$-IV code. When $n \not\equiv 0 \pmod{k-1}$, statement (3) is implied by statement (2). So suppose that $n \equiv 0 \pmod{k-1}$. Using instead a CPSA$(n, k; k-1)$ of size $B^{\circ}(n, k; k-1)$, adjoin the block $\{(k-1)s, (k-1)s+1, \ldots, (k-1)s+k-2, 0\}$. □

Lemma 3.5 $A^{II,IV}(n, 4, 3) \leq U(n, 3; 2)$ *when* $n \geq 13$.

Proof Computational results reported in Table 2 show that $A^{II,IV}(13, 4, 3) = U(13, 3; 2) = 16$, $A^{II,IV}(14, 4, 3) = U(14, 3; 2) = 20$, $A^{II,IV}(15, 4, 3) = U(15, 3; 2) = 25$, and

Table 2 Sizes of optimal codes for $n \leq 20$

n	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
$D(n, 3)$	1	1	2	4	7	8	12	13	17	20	26	28	35	37	44	48	57	60
$B(n, 3)$	0	0	1	2	4	6	9	10	14	16	21	24	30	32	39	42	50	54
$B^{\circ}(n, 3)$	0	0	0	2	3	5	9	10	13	16	20	23	30	32	38	42	49	53
$B(n, 3; 2)$	0	0	0	0	1	2	4	6	9	12	16	20	25	28	34	37	45	48
$B^{\circ}(n, 3; 2)$	0	0	0	0	0	0	3	5	8	12	15	18	25	26	34	36	43	46
$A^{II}.(n, 4, 3)$	1	1	2	4	5	6	9	10	14	16	21	*24*	*30*	*32*	*39*	*42*	*50*	*54*
$A^{III}(n, 4, 3)$	1	1	2	3	4	5	6	7	8	9	10	11	13	14	17	18	19	21
$A^{IV}(n, 4, 3)$	1	1	2	4	6	7	10	12	15	19	23	*26*	*32*	*35*	*42*	*45*	*54*	*57*
$A^{II,III}(n, 4, 3)$	1	1	2	3	3	4	5	6	7	8	10	11	13	13	17	18	19	20
$A^{II,IV}(n, 4, 3)$	1	1	2	4	4	4	7	8	12	13	16	20	25	28	34	37	45	48
$A^{III,IV}(n, 4, 3)$	1	1	2	3	4	5	6	7	8	9	10	11	13	14	17	18	19	21
$A^{II,III,IV}(n, 4, 3)$	1	1	2	3	3	4	5	6	7	8	10	11	13	13	17	18	19	20

Lower bounds and exact values

$A^{II,IV}(16,4,3) = U(16,3;2) = 32$. Suppose to the contrary that $A^{II,IV}(n,4,3) > U(n,3;2)$ for some $n \geq 17$, and let n be the smallest such value. When $n \geq 17$ we have $U(n,3;2) \geq U(n-1,3;2)+3$ and $U(n,3;2) \geq U(n-3,3;2)+4$. (See Table 2 for small values.)

Let $(X, \mathcal{B})$ be the support of an $(n,4,3)$-{II,IV} code of size $A^{II,IV}(n,4,3)$. Some triple of $\mathcal{B}$ covers a pair of the form $\{a,b\} \in \{\{i,i+1\},\{i,i+2\}\}$ because it is not an LPSA$(n,3;2)$.

Case 1 Some element appears in at most one triple. Suppose that element i appears in no triple. Shorten the code by deleting coordinate i and delete the triples (if any) containing pairs $\{i-1,i+1\}$, $\{i-2,i+1\}$, and $\{i-1,i+2\}$. The result is a type II and IV code, so the given code has at most $A^{II,IV}(n-1,4,3)+3$ triples, a contradiction. Suppose now that element i appears in exactly one triple T. Then if $i \in \{0,n-1\}$, delete coordinate i and triple T to get a contradiction. If $i \in \{1,n-2\}$, delete coordinate i and delete triple T, along with triples containing $\{0,2\}$ and $\{0,3\}$ when $i=1$ or $\{n-4,n-1\}$ and $\{n-3,n-1\}$, to get a contradiction. So $2 \leq i \leq n-3$. If T contains neither $i-1$ nor $i+1$, then no triple contains both $i-1$ and $i+1$, because the code is type IV. Shorten by deleting coordinate i and delete triple T and the triples (if any) containing pairs $\{i-2,i+1\}$ and $\{i-1,i+2\}$, yielding a contradiction.

Otherwise, without loss of generality T also contains $i-1$ but does not contain $i+1$. But then if some triple T' contains $i-2$ and $i+1$, it cannot contain i. If T' does not also contain $i-1$, then we have $T \cap \{i-1,i,i+1\} = \{i-1,i\}$ and $T' \cap \{i-1,i,i+1\} = \{i+1\}$, which cannot happen in a type II code. So $T' = \{i-2,i,i+1\}$. Hence there are at most two triples among those containing pairs $\{i-1,i+1\}$, $\{i-2,i+1\}$, and $\{i-1,i+2\}$, so shorten as before.

Case 2 Some triple T satisfies $|T \cap \{i,i+1,i+2\}| = 2$ for some $0 \leq i \leq n-3$. Suppose that $\{a,b\} = T \cap \{i,i+1,i+2\}$ and let $\{c\} = \{i,i+1,i+2\} \setminus \{a,b\}$. There can be no triple containing c but neither a nor b, because the code is type II and type IV. So c is in exactly two triples, T' that contains a and T'' that contains b; only T contains both a and b. Applying the same argument to T' and T'', a and b each appear in exactly two triples. So there are only three triples (T, T', and T'') that contain a, b, or c. Shorten by deleting coordinate $i+1$ and the triples T, T', and T'' to obtain a contradiction.

Case 3 No triple T satisfies $|T \cap \{i,i+1,i+2\}| = 2$ for any $0 \leq i \leq n-3$. If a triple T satisfies $|T \cap \{i,i+1,i+2\}| = 3$ for some $0 \leq i \leq n-3$, equivalently it satisfies $|T \cap \{i+1,i+2,i+3\}| = 2$ for some $0 \leq i \leq n-4$ or $|T \cap \{i-1,i,i+1\}| = 2$ for some $1 \leq i \leq n-3$. Apply Case 2. Otherwise every triple T satisfies $|T \cap \{i,i+1,i+2\}| \leq 1$ for $0 \leq i \leq n-3$. But then $(X, \mathcal{B})$ is an LPSA$(n,3;2)$ and hence we have at most $B(n,3;2) \leq U(n,3;2)$ triples, the final contradiction. □

4 Optimal packing sampling plans

By Corollary 2.2, we have the upper bound:

$$U(n,3) = \left\lfloor \frac{2\left\lfloor\frac{n-2}{2}\right\rfloor + (n-2)\left\lfloor\frac{n-3}{2}\right\rfloor}{3} \right\rfloor = \begin{cases} \frac{n^2-4n+4}{6}, & \text{if } n \equiv 2 \pmod 6, \\ \frac{n^2-3n}{6}, & \text{if } n \equiv 3 \pmod 6, \\ \frac{n^2-4n}{6}, & \text{if } n \equiv 0, 4 \pmod 6, \\ \frac{n^2-3n-4}{6}, & \text{if } n \equiv 1, 5 \pmod 6. \end{cases}$$

Theorem 4.1 $B(n,3) = U(n,3)$ *for all* $n \geq 0$.

Proof When $n \equiv 3 \pmod 6$, Colbourn and Rosa [4] (and Colbourn and Ling [5]) construct a BSA$(n, 3)$ of size $\frac{n^2-3n}{6}$, which is an optimal LPSA$(n, 3)$. Because each point appears in $\frac{n-3}{2}$ blocks, we get an LPSA$(n-1, 3)$ of size $\frac{n^2-3n}{6} - \frac{n-3}{2} = \frac{(n-1)^2-4(n-1)+4}{6}$ by removing the point $n-1$ and all blocks containing it, which is optimal.

When $n \equiv 1, 5 \pmod 6$, Colbourn and Rosa [4] showed there exists an $(n, 3)$-packing of size $\frac{n^2-3n+2}{6}$, whose leave graph consists of a cycle of length $n-1$ and one isolated point. Assume $n-1$ is the isolated point. Remove the block $\{x, n-2, n-1\}$ for some $x \in [0, n-3]$; the result is an optimal LPSA$(n, 3)$. Now, $n-1$ appears in $\frac{n-3}{2}$ blocks. Removing $n-1$ and all blocks containing it from the optimal LPSA$(n, 3)$ constructed above, we obtain an LPSA$(n-1, 3)$ of size $\frac{n^2-3n-4}{6} - \frac{n-3}{2} = \frac{(n-1)^2-4(n-1)}{6}$, which is optimal. □

Theorem 4.2 *1.* $B^\circ(n, 3) = U(n, 3)$ *when* $n \equiv 0, 3, 4 \pmod 6$.
2. $B^\circ(n, 3) = U(n, 3) - 1$ *when* $n \equiv 1, 2, 5 \pmod 6$.

Proof The constructions in Theorem 4.1 yield a CPSA$(n, 3)$ with $\frac{n(n-3)}{6}$ blocks when $n \equiv 3 \pmod 6$ and with $\frac{n(n-4)}{6}$ blocks when $n \equiv 0, 4 \pmod 6$. A CPSA$(n, 3)$ can have at most $\left\lfloor \frac{n}{3} \left\lfloor \frac{n-3}{2} \right\rfloor \right\rfloor$ blocks, which equals $U(n, 3)$ when $n \equiv 0, 3, 4 \pmod 6$, so these are optimal.

When $n \equiv 2 \pmod 6$, $\left\lfloor \frac{n}{3} \left\lfloor \frac{n-3}{2} \right\rfloor \right\rfloor = U(n, 3) - 1$ so $B^\circ(n, 3) \le U(n, 3) - 1$. When $n \equiv 1, 5 \pmod 6$, if there were a CPSA$(n, 3)$ with $U(n, 3) = \frac{n^2-3n-4}{6}$ codewords, then the number of edges in the leave graph is $\frac{n(n-1)}{2} - \frac{3(n^2-3n-4)}{6} = n + 2$. The leave must be an n-cycle with two additional edges, but every vertex in the leave must have even degree, which cannot occur. So $B^\circ(n, 3) \le U(n, 3) - 1$. To establish equality when $n \equiv 1, 2, 5 \pmod 6$, remove the block $\{0, n-1, x\}$ from an LPSA$(n, 3)$ from Theorem 4.1. □

Lemma 4.3 $B^\circ(n, 3; 2) = B(n, 3; 2) = U(n, 3; 2)$ *whenever* $n \equiv 3, 5 \pmod 6$ *and* $n \ge 15$. $B^\circ(n, 3; 2) + 2 = B(n, 3; 2) = U(n, 3; 2)$ *whenever* $n \equiv 2, 4 \pmod 6$ *and* $n \ge 14$.

Proof Zhang and Chang [30] establish that whenever $n \ge 15$ and $n \equiv 3, 5 \pmod 6$, there is a BSA$(n, 3; 2)$ having $\frac{n(n-5)}{6}$ blocks; this is also an optimal CPSA$(n, 3; 2)$ *and* LPSA$(n, 3; 2)$. Now suppose that $n \ge 14$ and $n \equiv 2, 4 \pmod 6$. When $n \equiv 2 \pmod 6$, writing $n = 6t + 2$, $U(6t + 2, 3; 2) = (2t)(3t - 1)$. Delete element $6t + 2$ from a BSA$(6t + 3, 3; 2)$ with $(2t + 1)(3t - 1)$ blocks, removing $3t - 1$ blocks to obtain an LPSA$(6t + 2, 3; 2)$, which is therefore optimal. When $n \equiv 4 \pmod 6$, writing $n = 6t + 4$, $U(6t + 4, 3; 2) = t(6t + 2)$. Delete element $6t + 4$ from a BSA$(6t + 5, 3; 2)$ with $t(6t + 5)$ blocks, removing $3t$ blocks to obtain an LPSA$(6t + 4, 3; 2)$, which is therefore optimal. Remove the blocks $\{0, n-2, x\}$, $\{1, n-1, y\}$ for some x and y from the optimal LPSA$(n, 3; 2)$ constructed above to obtain an optimal CPSA$(n, 3; 2)$ when $n \equiv 2, 4 \pmod 6$. □

For $n = 6t$, $U(6t, 3) = 6t(t-1) + 1$, and $\left\lfloor \frac{6t}{3} \left\lfloor \frac{6t-5}{2} \right\rfloor \right\rfloor = 6t(t-1)$. For $n = 6t + 1$, $U(6t+1, 3) = t(6t-3)$, and $\left\lfloor \frac{6t+1}{3} \left\lfloor \frac{6t-4}{2} \right\rfloor \right\rfloor = t(6t-3) - 1$. However, if a CPSA$(6t+1, 3; 2)$ were to have $t(6t-3) - 1$ blocks, its leave must have $2(6t+1) + 1$ edges and every such graph with minimum degree 4 has two vertices of degree 5. Because all vertices in the leave must have even degree, no CPSA$(6t + 1, 3; 2)$ can exist with more than $t(6t - 3) - 2$ blocks.

We provide bounds to apply when $n \equiv 0, 1 \pmod 6$.

Lemma 4.4 $B(2n, 3; 2) \ge 4B(n, 3)$*, and* $B(2n + 1, 3; 2) \ge 4B(n, 3) + n - 2$*. In addition,* $B^\circ(2n, 3; 2) \ge 4B^\circ(n, 3)$*, and* $B^\circ(2n + 1, 3; 2) \ge 4B^\circ(n, 3) + n - 3$.

Proof Start with an LPSA$(n, 3)$ on $[0, n-1]$. We form an LPSA$(2n, 3; 2)$ on $[0, 2n-1]$. For each block $\{a, b, c\}$ in the LPSA, form four blocks $\{\{2a+\alpha, 2b+\beta, 2c+\gamma\} : \alpha, \beta, \gamma \in \{0, 1\}, \alpha+\beta+\gamma \equiv 0 \pmod 2\}$. The verification is straightforward. To form an LPSA$(2n+1, 3)$ on $[0, 2n]$, adjoin $\{\{2i, 2i+3, 2n\} : 0 \leq i \leq n-3\}$.

The construction for CPSAs is the same, except that one does not adjoin $\{0, 3, 2n\}$. □

5 Conclusion

Applying Theorem 3.1 with the results in Theorem 4.1, we have optimal $(n, 4, 3)$-II codes for all $n \geq 30$. By computer search (using `cliquer` [13] and hill-climbing (a variant of [24])), we determined the sizes of optimal LPSA$(n, 3; \alpha)$s, CPSA$(n, 3; \alpha)$s, and $(n, 4, 3)$ codes of lengths $n \leq 20$. The sizes are listed in Table 2 and corresponding optimal codes are available from the authors; those in slanted font are lower bounds from Theorem 3.1 and Lemma 3.4.

In this paper, we present the first memoryless transition bus-encoding technique for power minimization, error-correcting and elimination of crosstalk simultaneously. We establish the connection between codes avoiding crosstalk of each type with packing sampling plans avoiding adjacent units. Optimal codes of each type are constructed.

References

1. Bertozzi D., Benini L., de Micheli G.: Low power error resilient encoding for on-chip data buses. In: DATE'02: Proceedings of the Conference on Design. Automation and Test in Europe, pp. 102–109. IEEE Computer Society, Washington, DC (2002).
2. Bertozzi D. Benini L., Ricco B.: Energy-efficient and reliable low-swing signaling for on-chip buses based on redundant coding. In: ISCAS'02: Proceedings of the IEEE International Symposium on Circuits and Systems, vol. 1, pp. 93–96. IEEE Press, Piscataway, NJ (2002).
3. Chee Y.M., Colbourn C.J., Ling A.C.H.: Optimal memoryless encoding for low power off-chip data buses. In: ICCAD'06: Proceedings of the 2006 IEEE/ACM International Conference on Computer-Aided Design, pp. 369–374. ACM Press, New York (2006).
4. Colbourn C.J., Rosa A.: Quadratic leaves of maximal partial triple systems. Graphs Comb. **2**(4), 317–337 (1986).
5. Colbourn C.J., Ling A.C.H.: A class of partial triple systems with applications in survey sampling. Commun. Stat. Theory Methods **27**(4), 1009–1018 (1998).
6. Duan C., Tirumala A., Khatri S.P.: Analysis and avoidance of crosstalk in on-chip buses. In: Hot Interconnects'01: Proceedings of the 9th Annual Symposium on High-Performance Interconnects, pp. 133–138. IEEE, Piscataway (2001).
7. Dukes P.J., Ling A.C.H.: Existence of balanced sampling plans avoiding cyclic distances. Metrika **70**, 131–140 (2009).
8. Favalli M., Metra C.: Bus crosstalk fault-detection capabilities of error-detecting codes for on-line testing. IEEE Trans. Very Large Scale Integr. Syst. **7**, 392–396 (1999).
9. Hamming R.W.: Error detecting and error correcting codes. Bell Syst. Tech. J. **29**(2), 147–160 (1950).
10. Hedayat A.S., Rao C.R., Stufken J.: Sampling plans excluding contiguous units. J. Stat. Plan. Inference **19**(2), 159–170 (1988).
11. Ho R.: On-chip wires: Scaling and efficiency, Ph.D. dissertation, Department of Electrical Engineering, Stanford University, Palo Alto, CA (2003).
12. Khan Z., Arslan T., Erdogan A.T.: A dual low-power and crosstalk immune encoding scheme for system-on-chip buses. In: PATMOS'04: Proceedings of the 14th International Workshop on Power and Timing Modeling, Optimization and Simulation. Lecture Notes in Computer Science, vol. 3254, pp. 585–592. Springer, Berlin (2004).
13. Niskanen S., Östergård P.R.J.: Cliquer User's Guide, Version 1.0, Communications Laboratory, Helsinki University of Technology, Espoo. Tech. Rep. **T48**, (2003).
14. Patel K.N., Markov I.L.: Error-correction and crosstalk avoidance in DSM busses. IEEE Trans. Very Large Scale Integr. Syst. **12**(10), 1076–1080 (2004).

15. Ramprasad S., Shanbhag N.R., Hajj I.N.: A coding framework for low-power address and data busses. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **7**, 212–221 (1999).
16. Rossi D., van Dijk E.S., Kleihorst R.P., Nieuwland A.K., Metra C.: Coding scheme for low energy consumption fault-tolerant bus. In: IOLTW'02: Proceedings of the Eighth IEEE International On-Line Testing Workshop, pp. 8–12. IEEE Computer Society, Washington, DC (2002).
17. Rossi D., Cavallotti S., Metra C.: Error correcting codes for crosstalk effect minimization. In: DFT'03: Proceedings of the 18th IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems, pp. 257–266. IEEE Computer Society, Washington, DC (2003).
18. Rossi D., van Dijk E.S., Kleihorst R.P., Nieuwland, A.K., Metra, C.: Power consumption of fault tolerant codes: the active elements. In IOLTW'03: Proceedings of the Ninth IEEE International On-line Testing Workshop, pp. 61–67. IEEE Computer Society, Washington, DC (2003).
19. Samala N.K., Radhakrishnan D., Izadi B.: A novel deep sub-micron bus coding for low energy. In: ESA'04: Proceedings of the International Conference on Embedded Systems and Applications, pp. 25–30. CSREA Press, Leuven (2004).
20. Shannon C.E.: A mathematical theory of communications, Bell Syst. Tech. J. **27**(3), 379–423, 623–656 (1948).
21. Sotiriadis P.P., Chandrakasan A.: Bus energy minimization by transition pattern coding (TPC) in deep sub-micron technologies. In: ICCAD'00—Proceedings of the 2000 IEEE/ACM International Conference on Computer-Aided Design, pp. 322–327. IEEE, Piscataway, NJ (2000).
22. Stan M.R., Burleson W.P.: Bus-invert coding for low-power I/O. IEEE Trans. Very Large Scale Integr. Syst. **3**(1), 49–58 (1995).
23. Stan M.R., Burleson W.P.: Coding a terminated bus for low power. In: Great Lakes Symposium VLSI, pp. 70–73, Buffalo, NY (1995).
24. Stinson D.R.: Hill-climbing algorithms for the construction of combinatorial designs. In: Algorithms in Combinatorial Design Theory. Annals of Discrete Mathematics, vol. 26, pp. 321–334. Elsevier, North-Holland (1985).
25. Stufken J.: Combinatorial and statistical aspects of sampling plans to avoid the selection of adjacent units. J. Comb. Inf. Syst. Sci. **18**(1–2), 149–160 (1993).
26. Su C.L., Tsui C.Y., Despain A.M.: Saving power in the control path of embedded processors. IEEE Des. Comput. **11**, 24–30 (1994).
27. Subrahmanya P., Manimegalai R., Kamakoti V., Mutyam M.: A bus encoding technique for power and cross-talk minimization. In: VLSI Design 2004: 17th International Conference on VLSI Design, pp. 443–448. IEEE Computer Society, Xi'an (2004).
28. Victor B., Keutzer K.: Bus encoding to prevent crosstalk delay. In: ICCAD'01—Proceedings of the 2001 IEEE/ACM International Conference on Computer-Aided Design, pp. 57–63. IEEE, Piscataway, NJ (2001).
29. Wright J.H., Stufken J.: New balanced sampling plans excluding adjacent units. J. Stat. Plan. Inference **138**, 3326–3335 (2008).
30. Zhang J., Chang Y.X.: The spectrum of BSA(v, 3, λ; α) with $\alpha = 2, 3$. J. Comb. Des. **15**, 61–76 (2007).