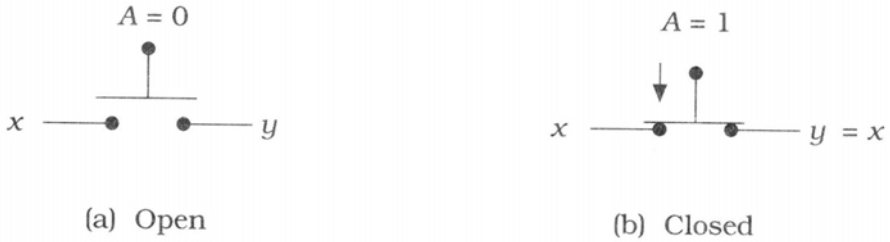
中国科学技术大学
University of Science and Technology of China

第 2 章 MOSFET逻辑设计

本章目录

§2.1 理想开关

1 高电平有效的控制开关



(a) Open (b) Closed

Figure 2.1 Behavior of an assert-high switch

2 低电平有效的控制开关

$y = x$

(a) Closed (b) Open

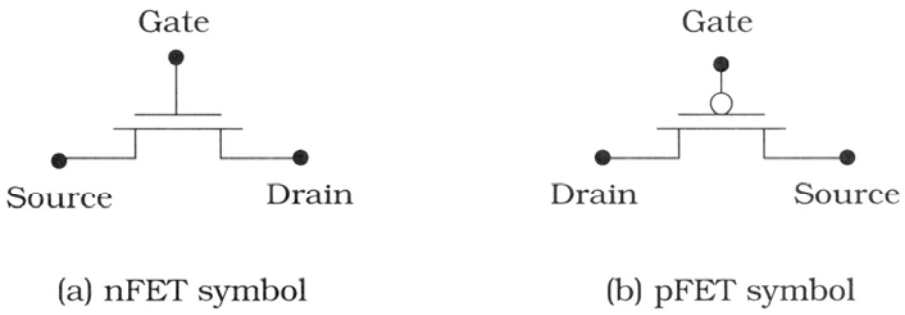
Figure 2.5 An assert-low switch

§2.2 MOSFET开关

1 MOSFET开关

MOSFET：金属氧化物半导体场效应晶体管

（metal-oxide-semiconductor field-effect transistor)



(a) nFET symbol　　(b) pFET symbol

Figure 2.9 Symbols used for nFETs and pFETs

- **栅极Gate，源极Source，漏极Drain。**
- **源极S、漏极D在物理上不是固定的，由工作时端电位决定。**

§2.2 MOSFET开关

2 布尔值与电参量之间的转换

（1） 双电源供电

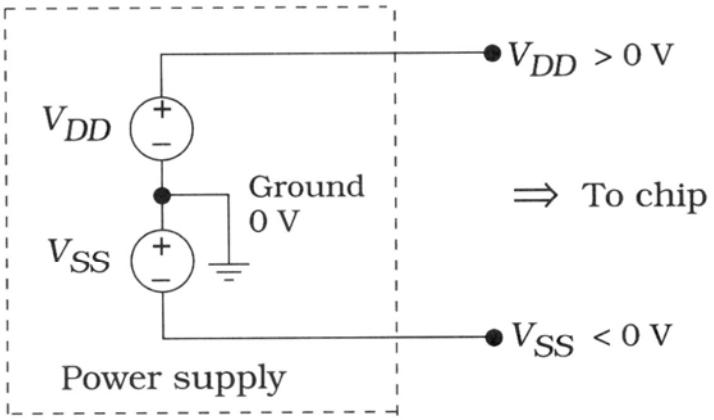


Figure 2.10 Dual power supply voltages

（2） 单电源供电

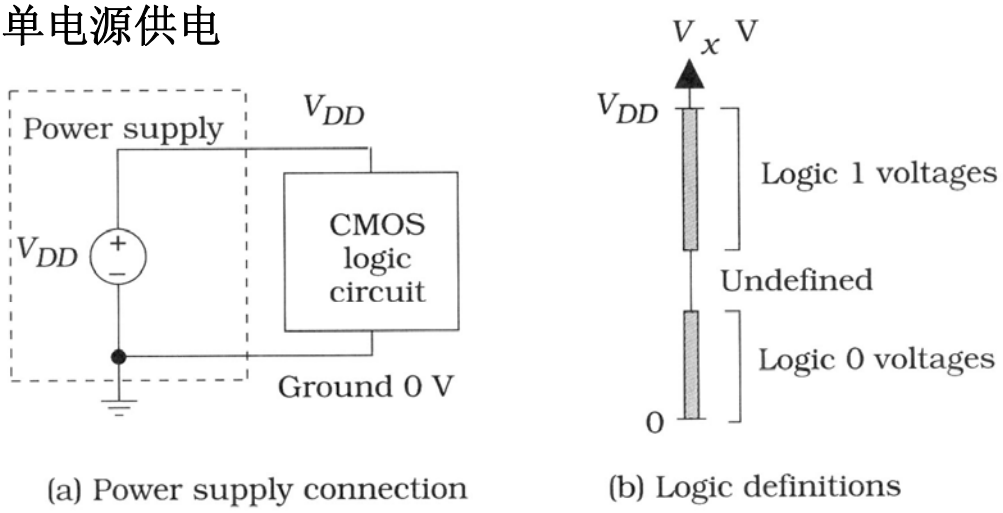


Figure 2.11 Single voltage power supply

正逻辑：高电平对应逻辑1，低电平对应逻辑0

负逻辑：高电平对应逻辑0，低电平对应逻辑1

3 MOSFET的开关特性

数字电路中，可将MOS管看作是由栅极信号控制的双向开关。

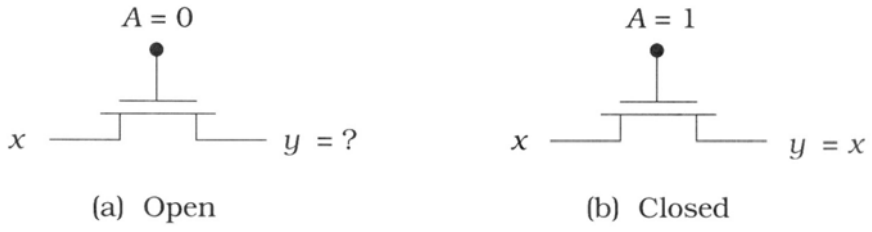


Figure 2.12 nFET switching characteristics

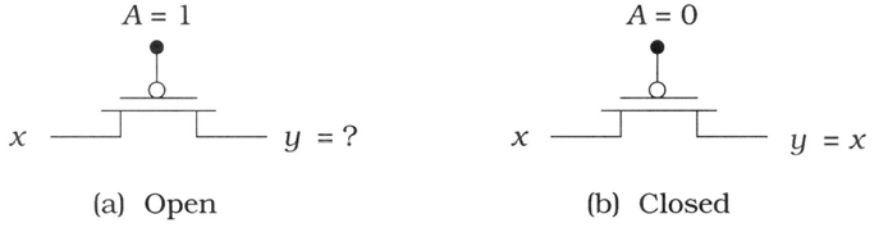


Figure 2.13 pFET switching characteristics

（1） 阈值电压V_T：开始形成导电沟道时的栅源电压。

NMOS： 阈值电压V_{Tn}为正数，典型值**0.3~0.7V**

$V_{GSn} > V_{Tn}$时，晶体管导通

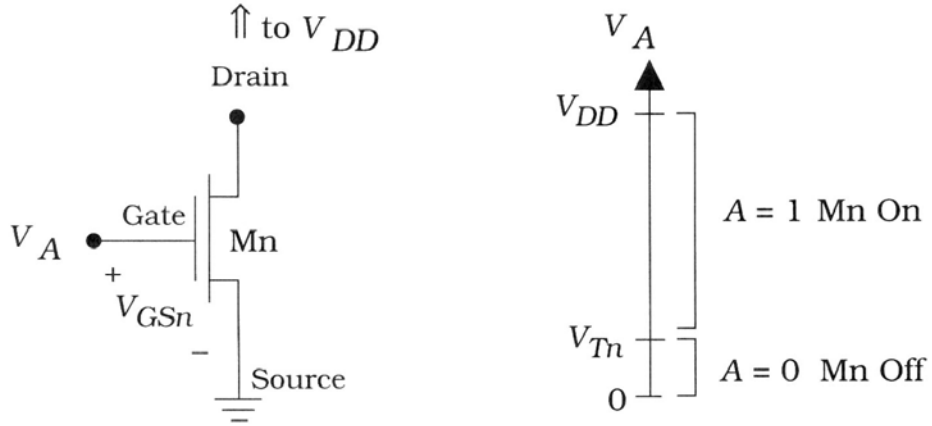
$V_{GSn} \leqslant V_{Tn}$时，晶体管截止

PMOS： 阈值电压V_{Tp}为负数，典型值**–0.3~ – 0.8V**

$V_{SGp} > |V_{Tp}|$时，晶体管导通

$V_{SGp} \leqslant |V_{Tp}|$时，晶体管截止

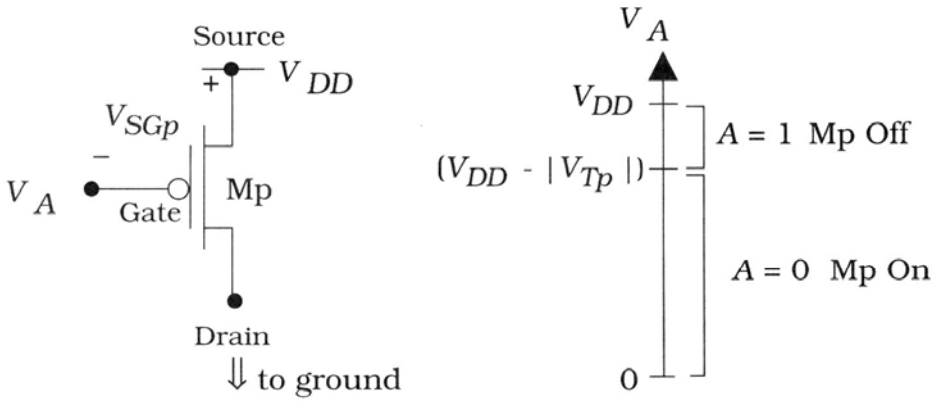
NMOS阈值电压V_{Tn}逻辑含义



(a) Gate-source voltage (b) Logic translation

Figure 2.14 Threshold voltage of an nFET

PMOS阈值电压V_{Tp}逻辑含义

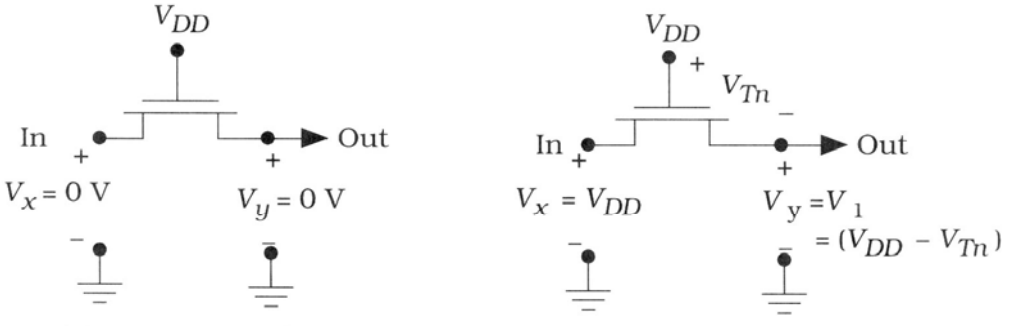


(a) Source-gate voltage (b) Logic translation

Figure 2.15 pFET threshold voltage

（2） 电压传输特性

NMOS电压传输特性：



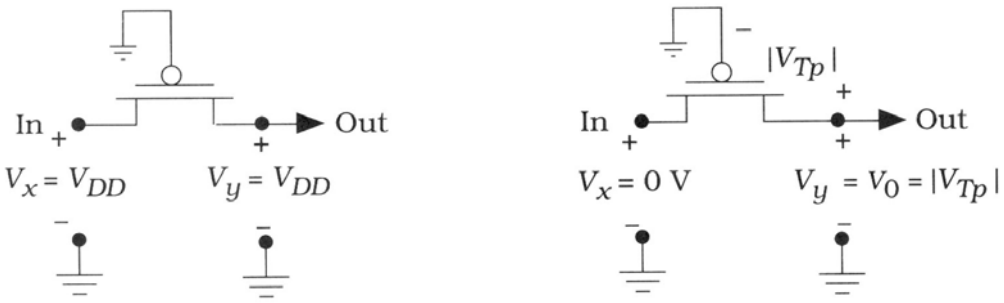
(a) Logic 0 transfer (b) Logic 1 transfer

Figure 2.16 nFET pass characteristics

NMOS传送强逻辑0电压，但传送弱逻辑1电压

§ 2.2 MOSFET开关

PMOS电压传输特性：



(a) Logic 1 transfer　　(b) Logic 0 transfer

Figure 2.17 pFET pass characteristics

PMOS传送强逻辑1电压，但传送弱逻辑0电压

如何解决传送电平时阈值电压损失（**Threshold Drops**）问题？

设计互补MOS（CMOS）解决传送电平问题，用PMOS传送逻辑1，用NMOS传送逻辑0

§ 2.3 基本的CMOS逻辑门

1 CMOS逻辑门的结构

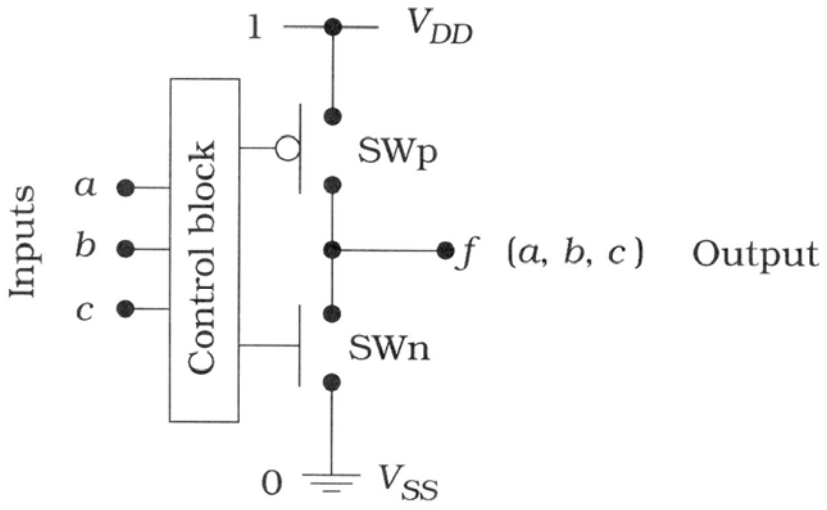


Figure 2.18 General CMOS logic gate

CMOS逻辑门的工作情况

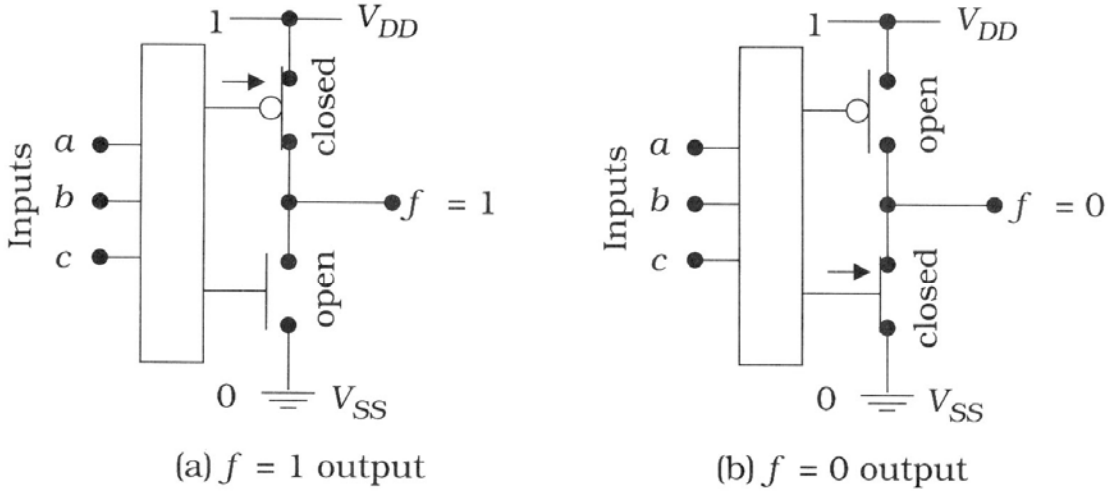


Figure 2.19 Operation of a CMOS logic gate

2 互补对

互补对由一个**NMOS**和一个**PMOS**组成，它们的栅极连在一起

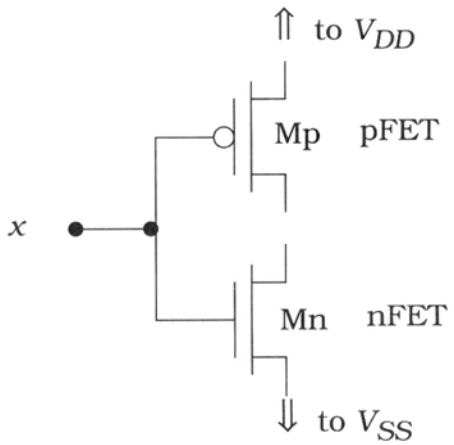
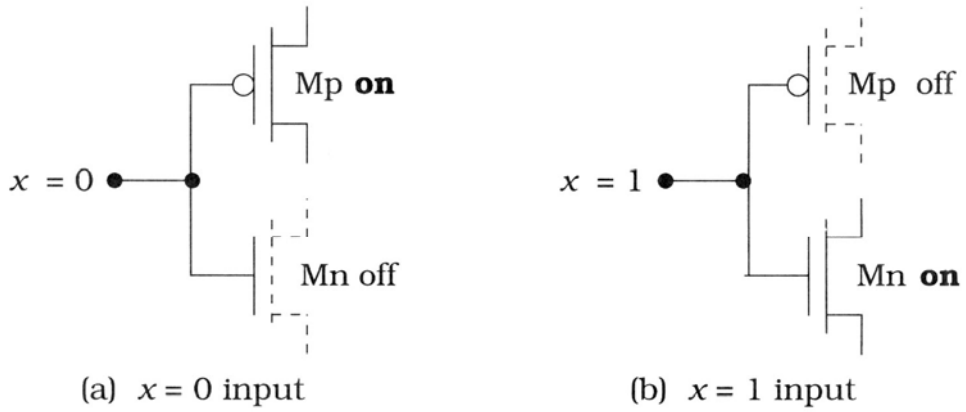


Figure 2.20 A CMOS complementary pair

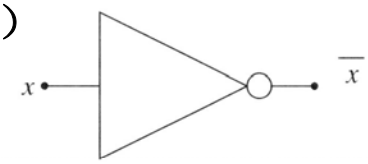
互补对的工作情况



(a) $x = 0$ input (b) $x = 1$ input

Figure 2.21 Operation of the complementary pair

2.3.1 非门（反相器）



x	$\overline{x}$
0	1
1	0

(a) Logic symbol (b) Truth table

Figure 2.22 NOT gate

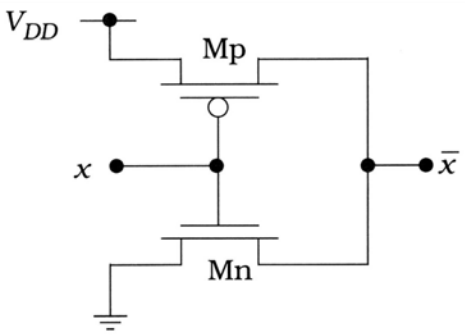
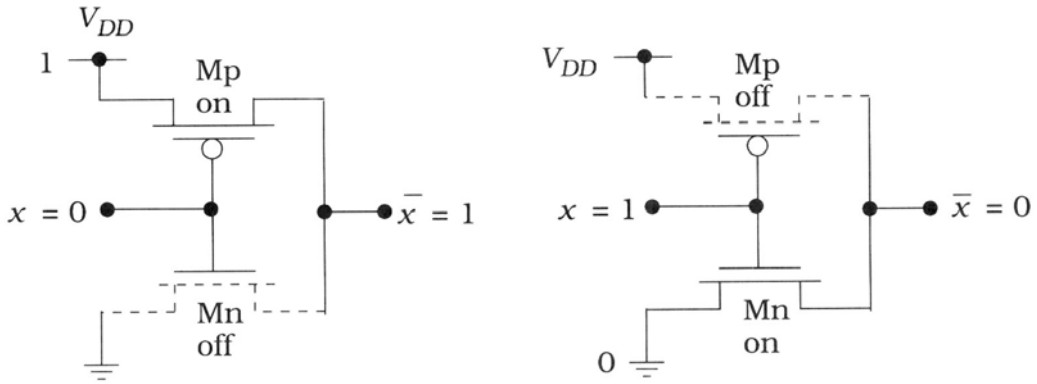


Figure 2.23 CMOS NOT gate

CMOS反相器的工作情况

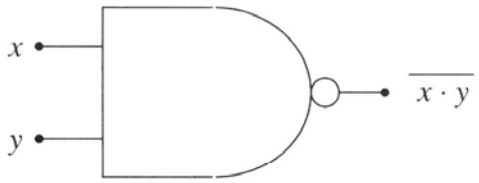


(a) $x = 0$ input (b) $x = 1$ input

Figure 2.24 Operation of the CMOS NOT gate

2.3.3 与非门

逻辑符号与真值表

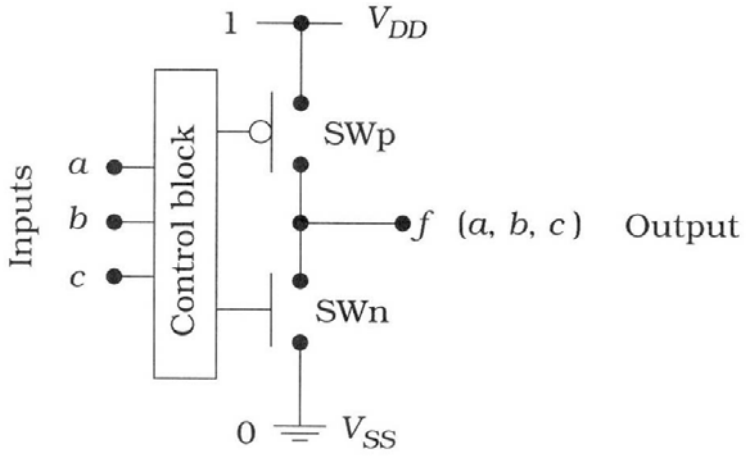


x	y	$\overline{x \cdot y}$
0	0	1
0	1	1
1	0	1
1	1	0

(a) Logic symbol (b) Truth table

Figure 2.31 NAND2 logic gate

§2.3 基本的CMOS逻辑门



设计原理：

☞对每个输入使用一个NMOS/PMOS互补对

☞将输出节点通过PMOS与电源V_{DD}相连

☞将输出节点通过NMOS与地相连

☞确保输出总是一个正确定义的高电平或低电平

§2.3 基本的CMOS逻辑门

CMOS NAND2逻辑电路

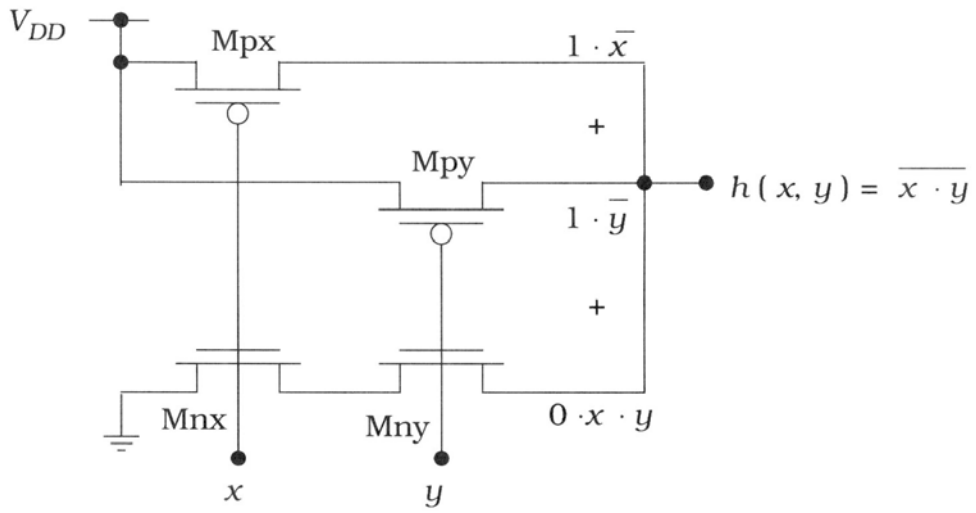


Figure 2.34 CMOS NAND2 logic circuit

CMOS NAND3逻辑电路

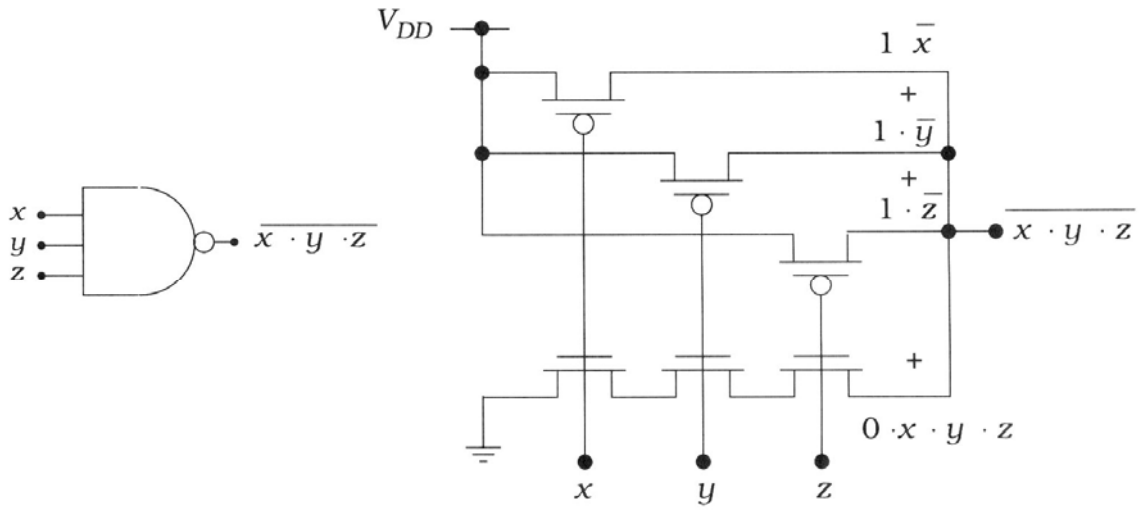
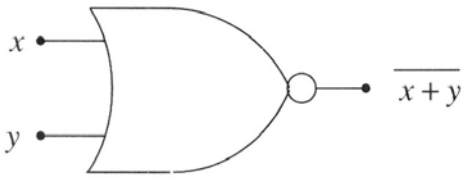


Figure 2.36 A NAND3 logic gate in CMOS

2.3.2 或非门

逻辑符号与真值表



x	y	$\overline{x+y}$
0	0	1
0	1	0
1	0	0
1	1	0

(a) Logic symbol (b) Truth table

Figure 2.25 NOR logic gate

CMOS NOR2逻辑电路

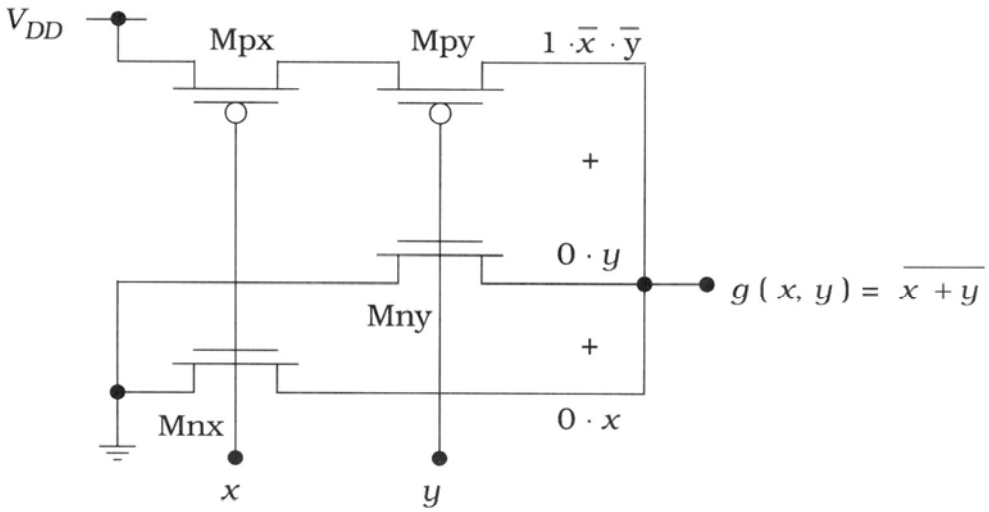


Figure 2.28 CMOS NOR2 gate

CMOS NOR3逻辑电路

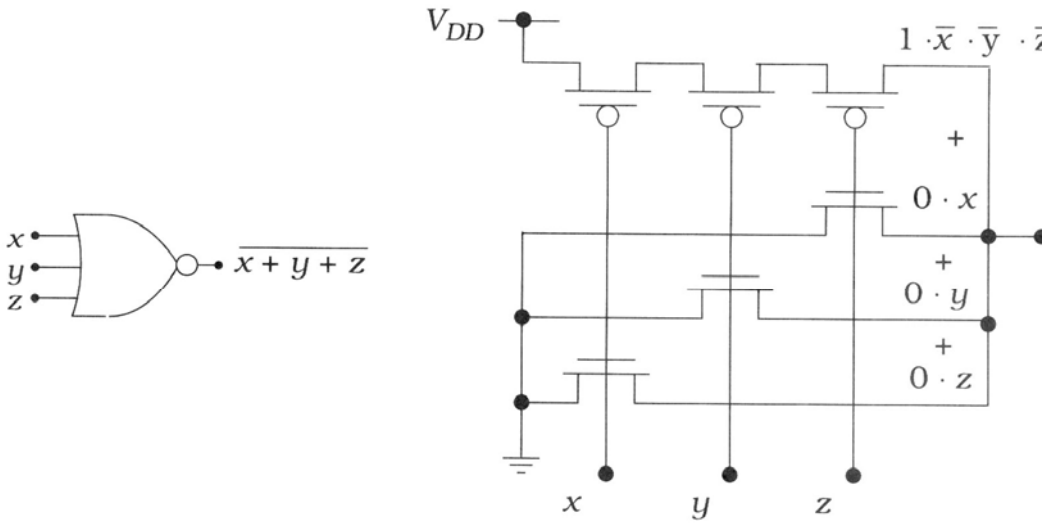


Figure 2.30 A NOR3 gate in CMOS

§ 2.3 基本的CMOS逻辑门

思考：

1 在IC中，并不采用NAND3 、 NOR3类似结构实现5输入以上的与非门和或非门，为什么？

2 PMOS和NMOS两个网络实现的逻辑功能一致，能否省去其中一个？

§ 2.4 CMOS复合逻辑门

复合逻辑门：实现几个最基本逻辑操作组合的单个电路。

- 与或非门AOI
- 或与非门OAI

例：$F = \overline{a \cdot (b + c)}$

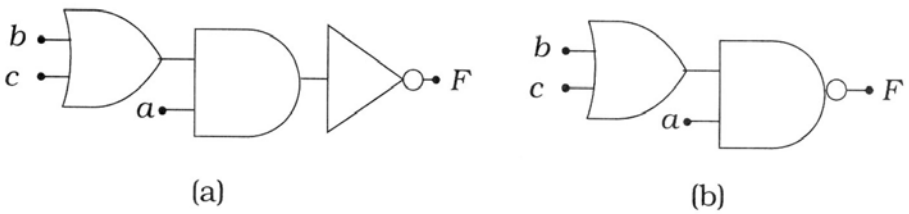


Figure 2.37 Logic function example

§2.4 CMOS复合逻辑门

例：$F=\overline{a\cdot(b+c)}$

PMOS网络

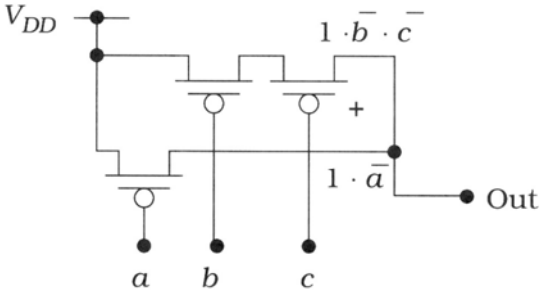


Figure 2.38 pFET circuit for F from equation (2.51)

NMOS网络

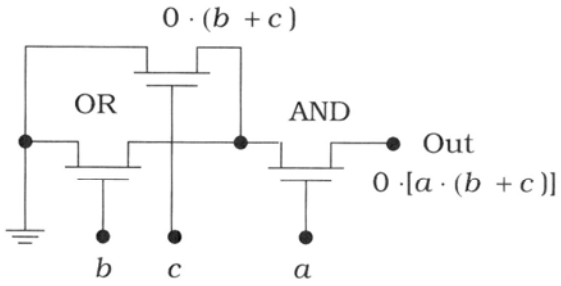


Figure 2.39 nFET logic circuit for F

§2.4 CMOS复合逻辑门

最终完成的CMOS复合逻辑门电路

例：$F=\overline{a\cdot(b+c)}$

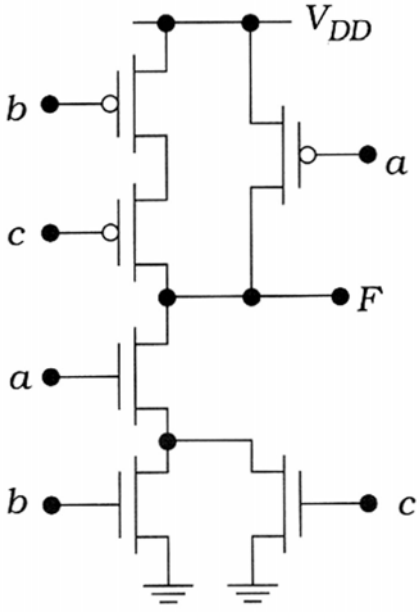


Figure 2.41 Finished complex CMOS logic gate circuit

§ 2.4.1 结构化逻辑设计

CMOS逻辑门本质上是反相的

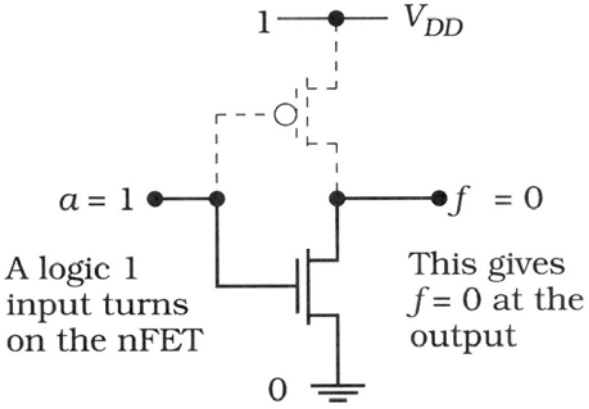


Figure 2.42 Origin of the inverting characteristic of CMOS gates

NMOS形成逻辑的特点：

串联NMOS实现“与非”逻辑

并联NMOS实现“或非”逻辑

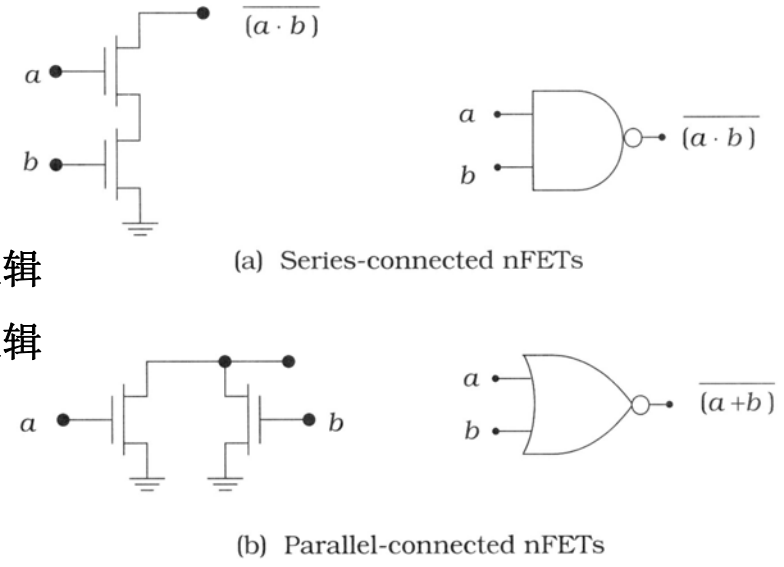


Figure 2.43 nFET logic formation

§2.4 CMOS复合逻辑门

串联和并联NMOS的组合可实现复合逻辑门

NMOS AOI 电路： $X = \overline{a \cdot b + c \cdot d}$

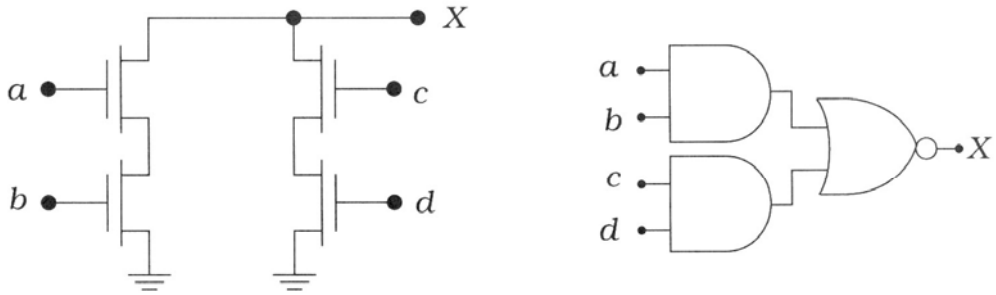


Figure 2.44 nFET AOI circuit

§2.4 CMOS复合逻辑门

NMOS OAI 电路： $Y = \overline{(a+e)\cdot(b+f)}$

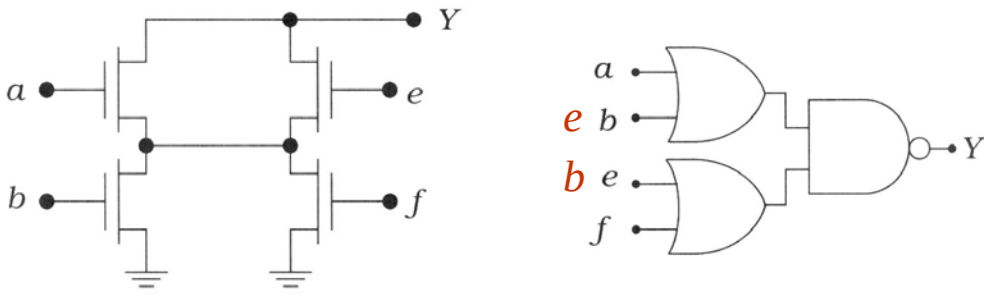
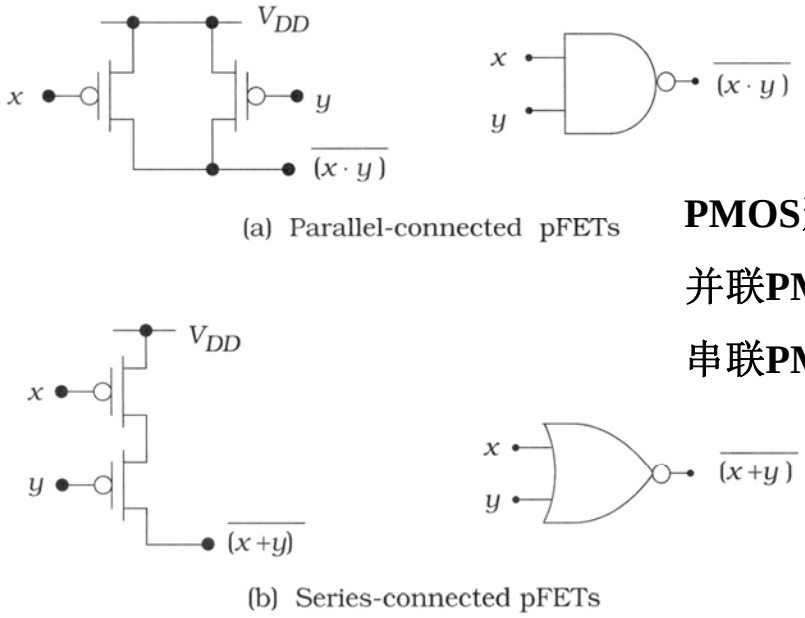


Figure 2.45 nFET OAI network



PMOS形成逻辑的特点：

并联PMOS实现“与非”逻辑

串联PMOS实现“或非”逻辑

Figure 2.46 pFET logic formation

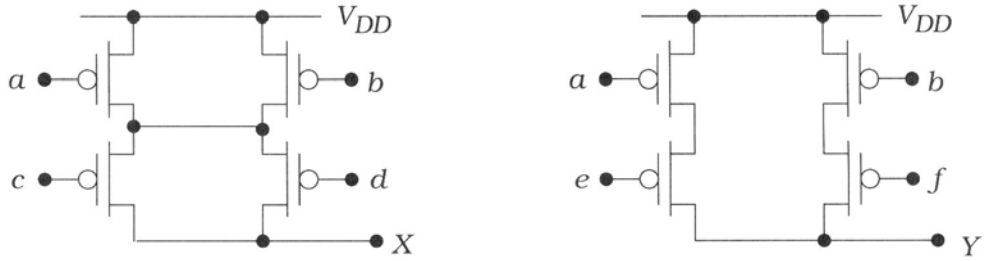
串联和并联PMOS的组合可实现复合逻辑门

PMOS AOI 电路：

$$X = \overline{a \cdot b + c \cdot d}$$

PMOS OAI 电路：

$$Y = \overline{(a+e) \cdot (b+f)}$$



(a) pFET AOI circuit (b) pFET OAI circuit

Figure 2.47 pFET arrays for AOI and OAI gates

§ 2.4 CMOS复合逻辑门

完整的CMOS AOI和OAI电路

$X = \overline{a \cdot b + c \cdot d}$　　$Y = \overline{(a+e)\cdot(b+f)}$

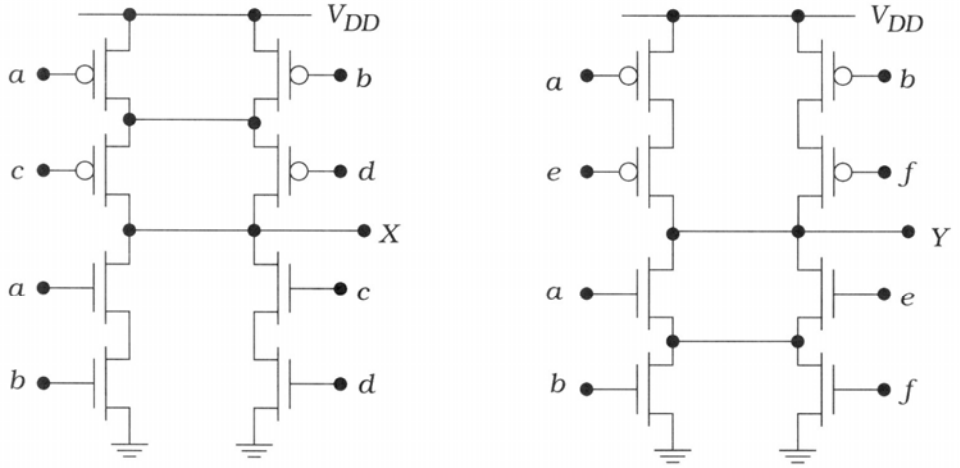


Figure 2.48 Complete CMOS AOI and OAI circuits

§ 2.4 CMOS复合逻辑门

例2.1 实现复合逻辑门 $X = \overline{a + b \cdot (c+d)}$

NMOS电路的实现：

第一组：输入为*c*和*d*的NMOS并联；

第二组：输入为*b*的一个NMOS和第一组串联；

第三组：输入为*a*的一个NMOS和第二组并联。

PMOS电路的实现：

第一组：输入为*c*和*d*的PMOS串联；

第二组：输入为*b*的一个PMOS和第一组PMOS并联；

第三组：输入为*a*的一个PMOS和第二组PMOS串联。

§ 2.4 CMOS复合逻辑门

完整的电路

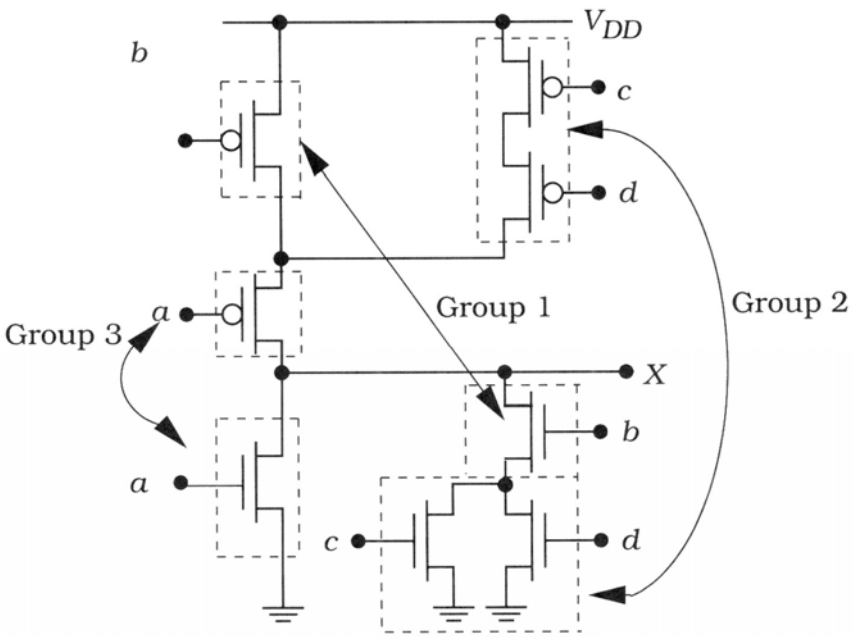
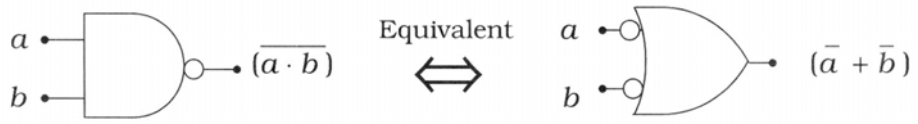


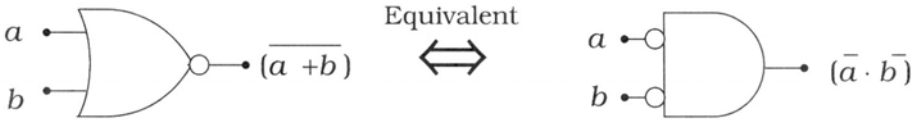
Figure 2.49 AOI circuit for Example 2.1

§ 2.4 CMOS复合逻辑门

移动反相小圈的方法



(a) NAND - OR



(b) NOR - AND

Figure 2.52 Bubble pushing using DeMorgan rules

理论基础：**Demorgan**定理

例2.2 实现复合逻辑门 $G = \overline{ab + cd + e}$

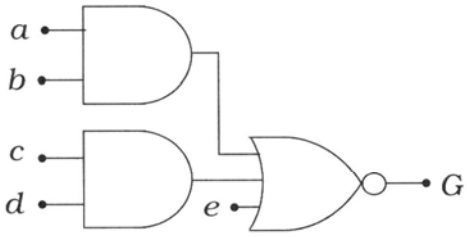
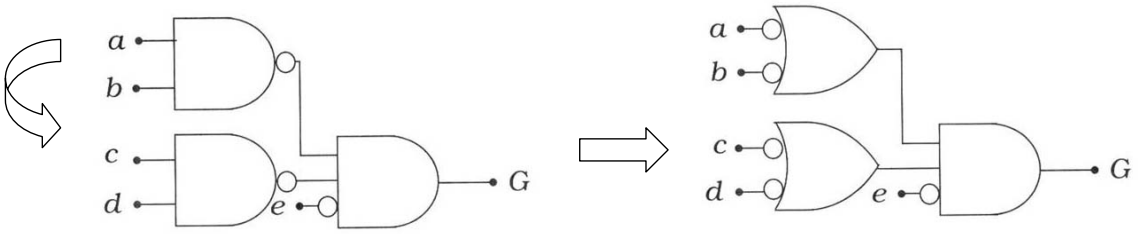


Figure 2.53 AOI logic diagram for bubble-pushing example



(a) First transformation　　(b) Final form

完整的电路

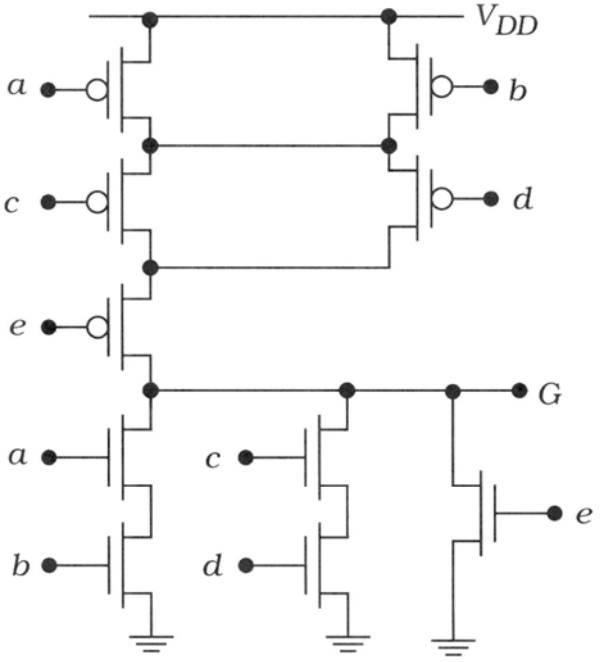


Figure 2.55 Final circuit for the bubble-pushing example

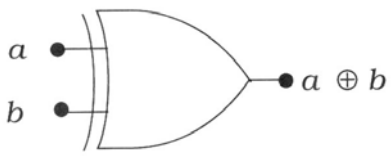
§2.4 CMOS复合逻辑门

CMOS逻辑门的晶体管电路设计步骤：

- **用基本的AOI或OAI结构构成电路图。允许如OAOI和AOAI这样的深层嵌套；**
- **在输出和地之间构成NMOS逻辑电路：**
  串联NMOS提供“与非”操作，并联NMOS提供“或非”操作；
- **在输出和V_{DD}之间构成PMOS逻辑电路：**
  （1）PMOS和NMOS网络结构对偶：NMOS串联——PMOS并联，NMOS并联——PMOS串联
  （2）将小圈推回输入端，可得到PMOS网络的连接拓扑。

§2.4 CMOS复合逻辑门

§2.4.2 异或门（XOR）和异或非门（XNOR）



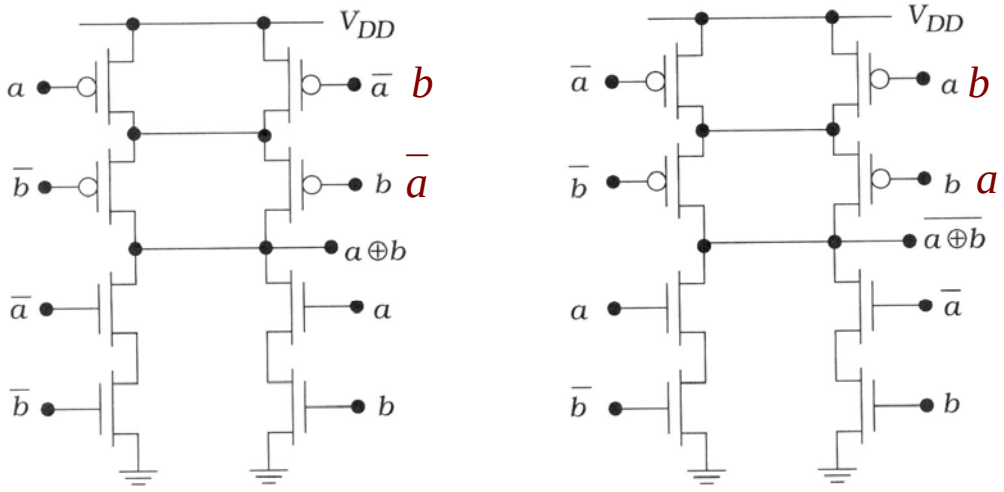
a	b	$a \oplus b$
0	0	0
0	1	1
1	0	1
1	1	0

Figure 2.56 Exclusive-OR (XOR) symbol and truth table

异或门：$a \oplus b = \bar{a} \cdot b + a \cdot \bar{b} = \overline{a \cdot b + \bar{a} \cdot \bar{b}}$

异或非门：$\overline{a \oplus b} = a \cdot b + \bar{a} \cdot \bar{b} = \overline{\bar{a} \cdot b + a \cdot \bar{b}}$

异或门（XOR）和异或非门（XNOR）的电路

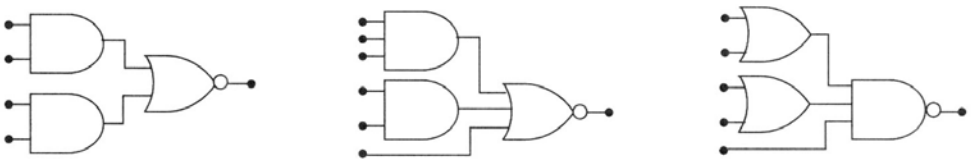


(a) Exclusive-OR　　(b) Exclusive-NOR

Figure 2.57 AOI XOR and XNOR gates

§ 2.4.3 一般化的AOI和OAI逻辑门

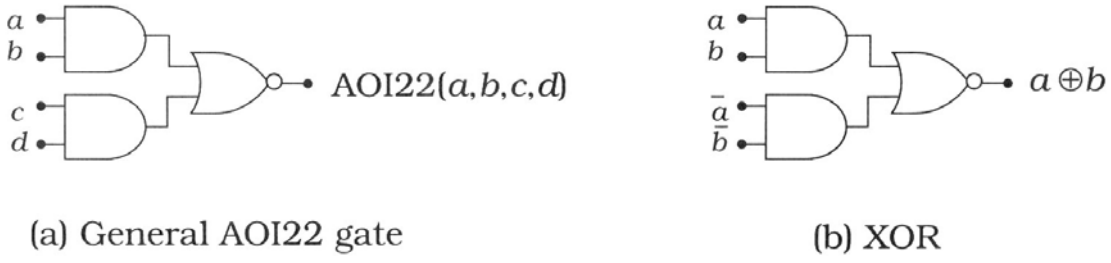
命名方法：



(a) AOI22 gate　(b) AOI321 gate　(c) OAI221 gate

Figure 2.58 General naming convention

§2.4 CMOS复合逻辑门



(a) General AOI22 gate　　(b) XOR

Figure 2.59 Application of an AOI22 gate

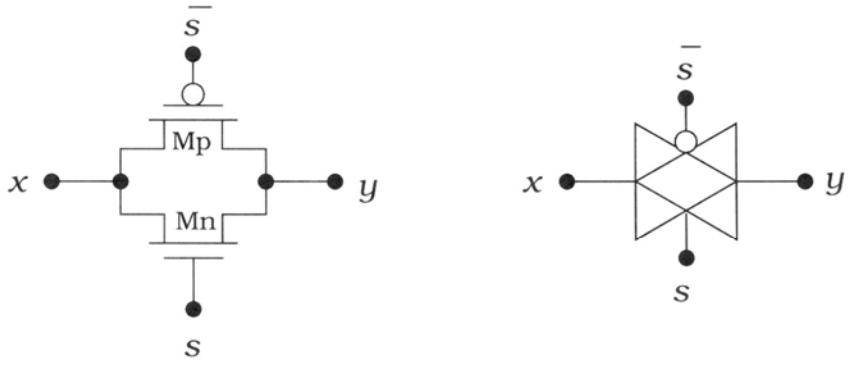
例：$\mathrm{AOI22}(a,b,c,d)=\overline{ab+cd}$

$a\oplus b=\mathrm{AOI22}(a,b,\bar{a},\bar{b})$

$\overline{a\oplus b}=\mathrm{AOI22}(a,\bar{b},\bar{a},b)$

§2.5 传输门(TG)电路

CMOS传输门：一个NMOS和PMOS并联构成



(a) Transistor circuit　　(b) Symbol

Figure 2.60 Transmission gate (TG)

优点：可传送全范围电压 **[0，V_{DD}]**

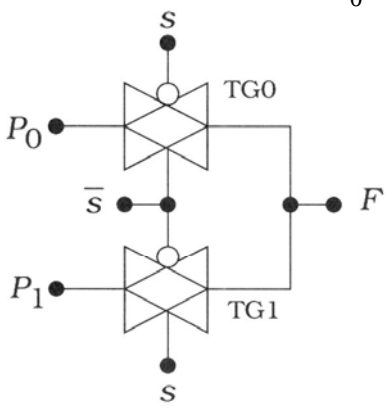
缺点：需要两个**MOSFET**和一个反相器

§ 2.5 传输门(TG)电路

传输门的逻辑设计

1 多路选择器（MUX）

$$2:1\text{MUX}: \qquad F = P_0 \cdot \bar{s} + P_1 \cdot s$$



s	TG0	TG1	F
0	Closed	Open	P_0
1	Open	Closed	P_1

Figure 2.61 A TG-based 2-to-1 multiplexor

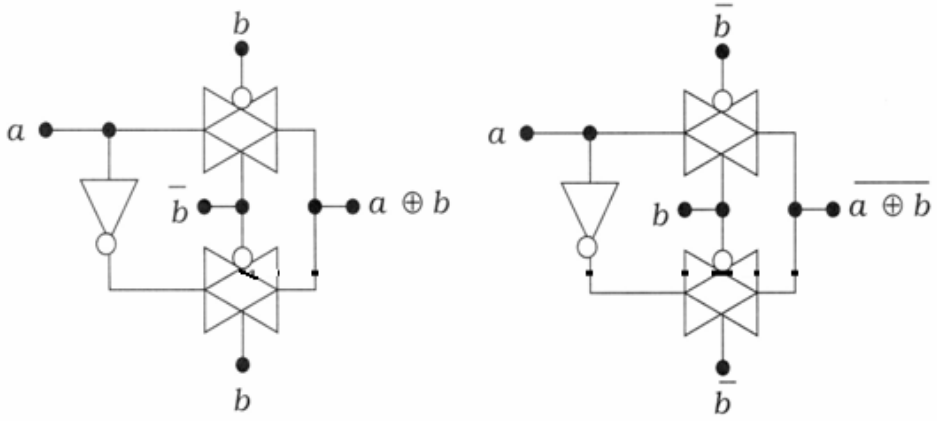
怎样扩展为4:1MUX？

§ 2.5 传输门(TG)电路

用2:1MUX设计XOR和XNOR（6+2个MOSFET）

$$2:1\text{MUX}: \qquad F = P_0 \cdot \bar{s} + P_1 \cdot s$$

$$a \oplus b = a \cdot \bar{b} + \bar{a} \cdot b \qquad \overline{a \oplus b} = a \cdot b + \bar{a} \cdot \bar{b}$$

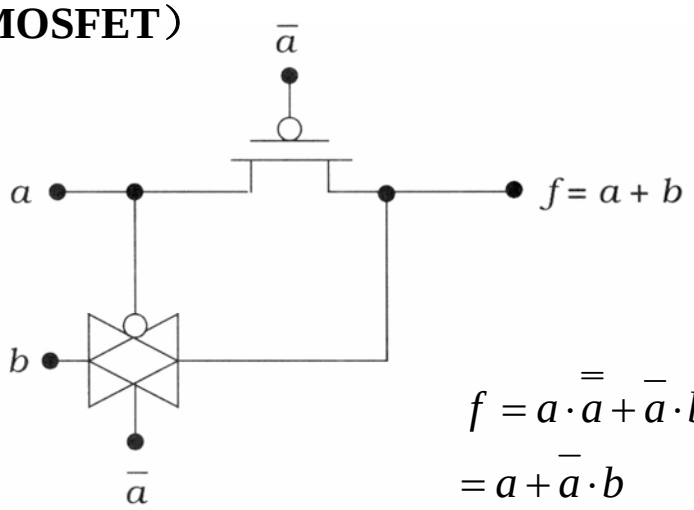


(a) XOR circuit (b) XNOR circuit

Figure 2.62 TG-based exclusive-OR and exclusive-NOR circuits

§2.5 传输门(TG)电路

2 或门（3+2个MOSFET）



$$f = a \cdot \overline{a} + \overline{a} \cdot b$$
$$= a + \overline{a} \cdot b$$
$$= a + b$$

Figure 2.63 A TG-based OR gate

如何用5个FET构造AND门？

§2.5 传输门(TG)电路

3 另一种XOR和XNOR电路（4+2个MOSFET）

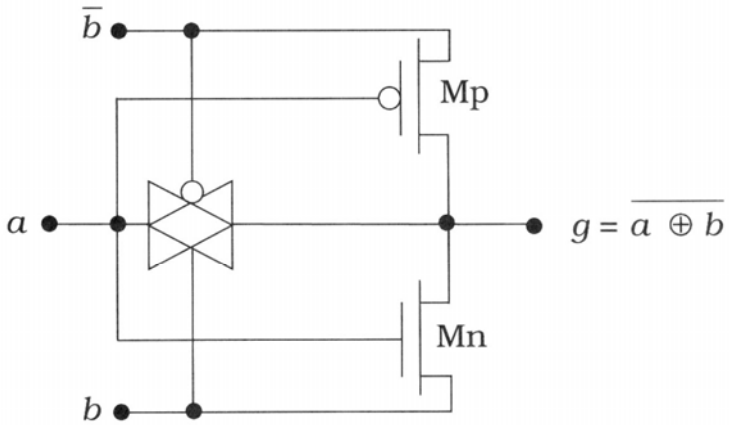
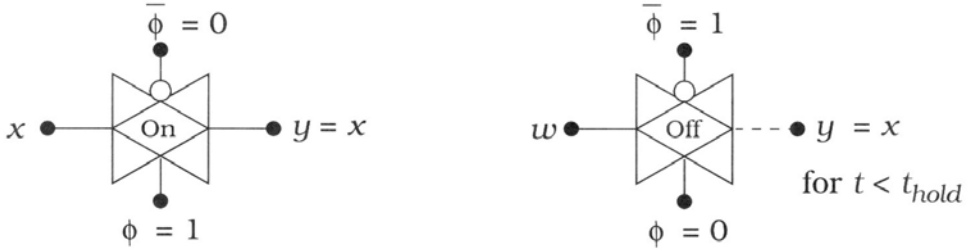


Figure 2.64 An XNOR gate that uses both TGs and FETs

1 时钟控制的传输门



(a) Closed switch (b) Open switch

Figure 2.66 Behavior of a clocked TG

2 用传输门实现数据同步

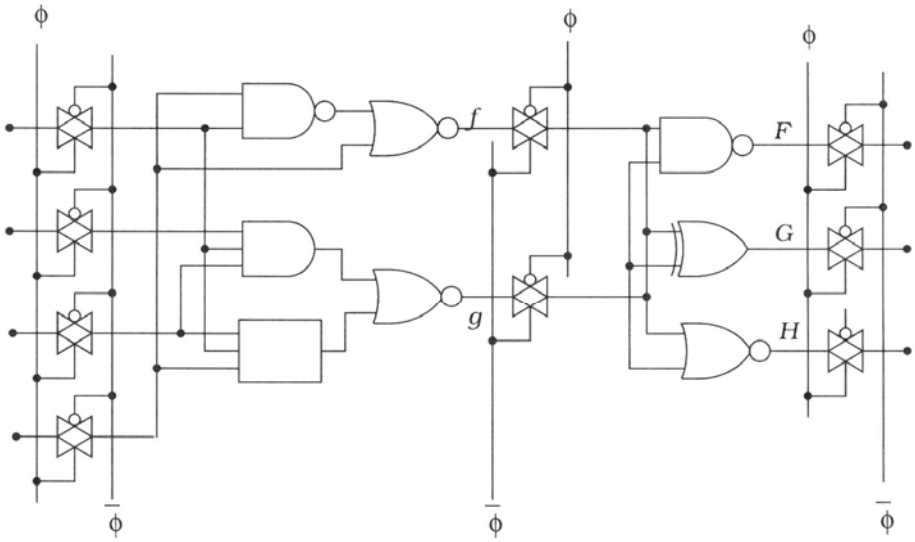


Figure 2.67 Data synchronization using transmission gates

模块级系统时序图

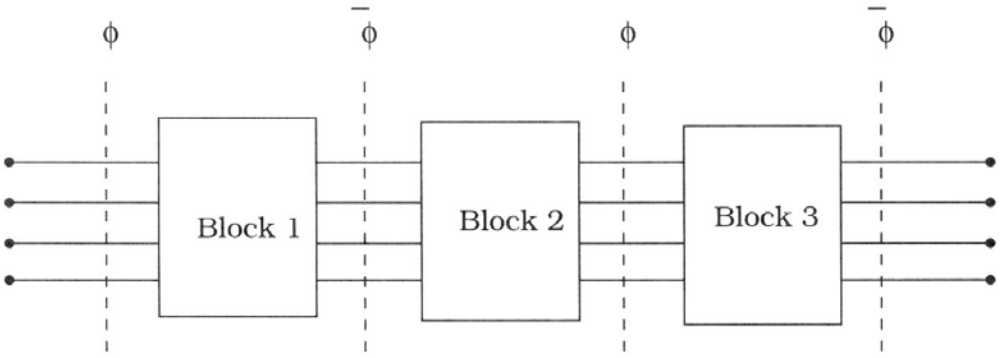


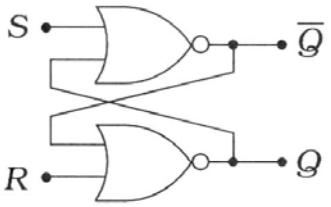
Figure 2.68 Block-level system timing diagram

$$T/2 < t_{\text{hold}}$$

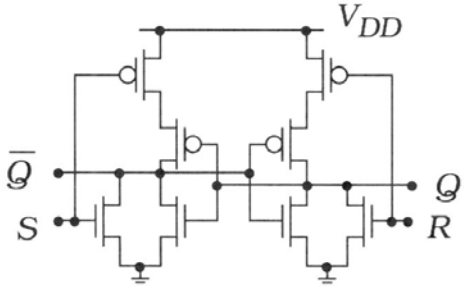
3 锁存器

若长时间保存数据，需用锁存器

SR锁存器



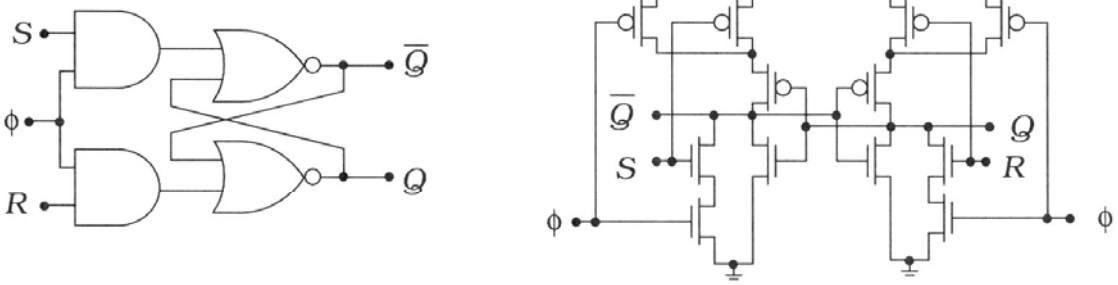
(a) Logic diagram



(b) CMOS circuit

Figure 2.70 SR latch

钟控SR锁存器



(a) Logic diagram　　(b) CMOS circuit

Figure 2.71 Clocked SR latch