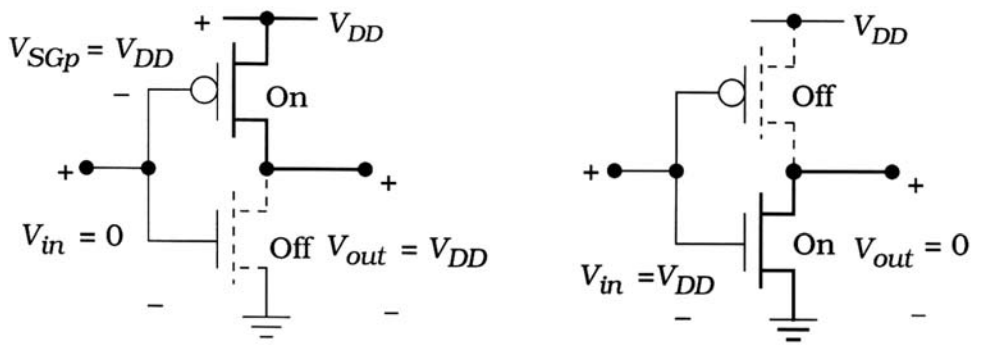
中国科学技术大学
University of Science and Technology of China

第 7 章 CMOS逻辑门电子学分析

本章目录

§7.1 CMOS反相器的直流特性

1 逻辑摆幅V_L



(a) Low input voltage (b) High input voltage

Figure 7.2 V_{OH} and V_{OL} for the inverter circuit

输出高电压：$V_{OH,max}=V_{DD}$ 输出低电压：$V_{OL,min}=0V$

逻辑摆幅：$V_L=V_{OH,max}-V_{OL,min}=V_{DD}$

逻辑摆幅等于全部电源电压值，称为全轨输出。

全轨输出：**full-rail output** 或 **rail to rail output**

§7.1 CMOS反相器的直流特性

2 电压传输特性曲线（VTC）

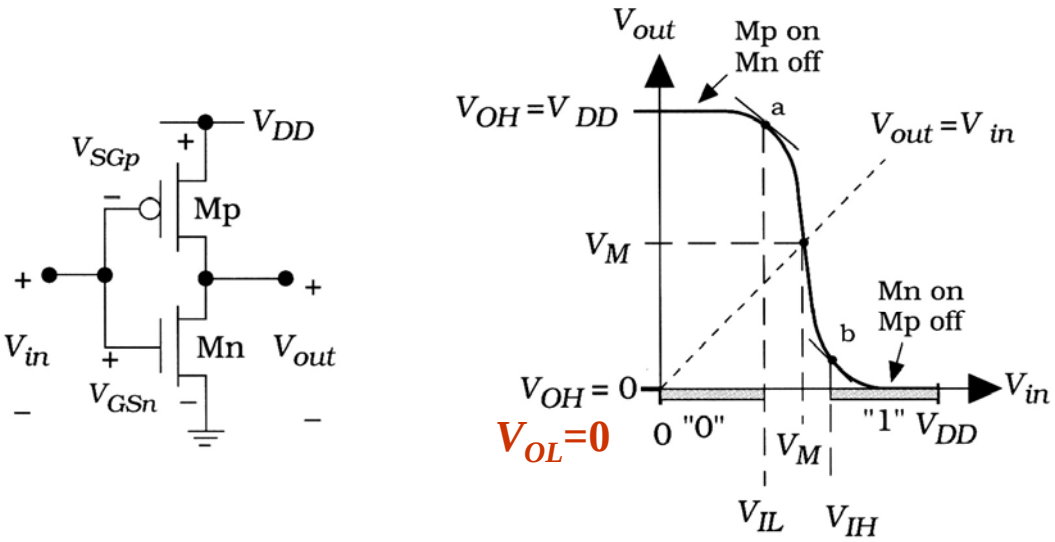
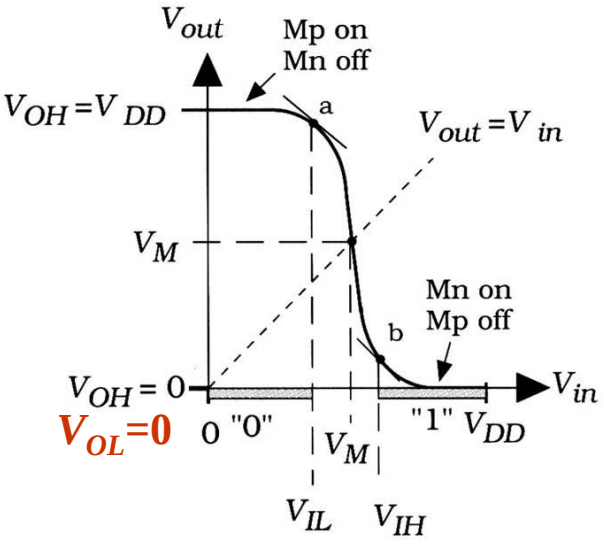


Figure 7.3 Voltage transfer curve for the NOT gate

§7.1 CMOS反相器的直流特性

2 电压传输特性曲线（VTC）——可分为5个区域



A区，$0 \le V_{in} < V_{Tn}$：

NMOS截止，PMOS导通；

B区，$V_{Tn} < V_{in} < V_{out} - |V_{Tp}|$：

NMOS饱和，PMOS非饱和；

C区，$V_{out} - |V_{Tp}| < V_{in} < V_{out} + V_{Tn}$：

NMOS饱和，PMOS饱和；

D区，$V_{out} + V_{Tn} < V_{in} < V_{DD} - |V_{Tp}|$：

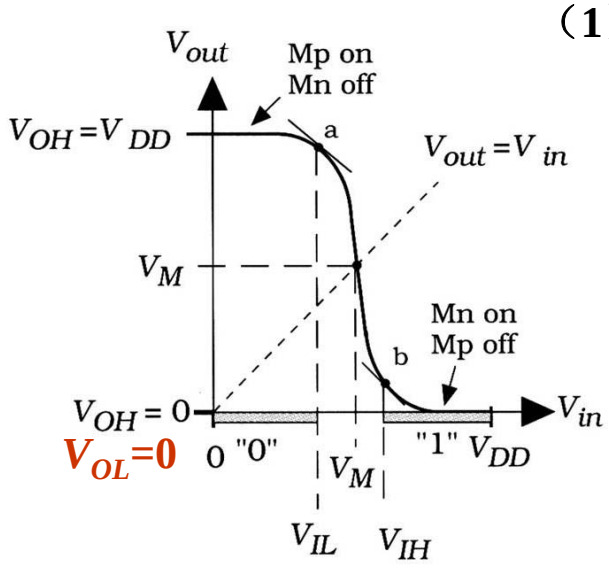
NMOS非饱和，PMOS饱和；

E区，$V_{DD} - |V_{Tp}| < V_{in} \le V_{DD}$：

NMOS导通，PMOS截止。

§ 7.1 CMOS反相器的直流特性

2 电压传输特性曲线（VTC）



（1）输入低电压和输入高电压

$$V_{out}=f(V_{in})$$

$$令\ \frac{dV_{out}}{dV_{in}}=-1$$

逻辑0的输入电压范围：

$$0\le V_{in}\le V_{IL}$$

逻辑1的输入电压范围：

$$V_{IH}\le V_{in}\le V_{DD}$$

§ 7.1 CMOS反相器的直流特性

2 电压传输特性曲线（VTC）

a点坐标：

$$\frac{1}{2}\beta_n(V_{in}-V_{Tn})^2=\frac{1}{2}\beta_p[2(V_{DD}-V_{in}-|V_{Tp}|)(V_{DD}-V_{out})-(V_{DD}-V_{out})^2]$$

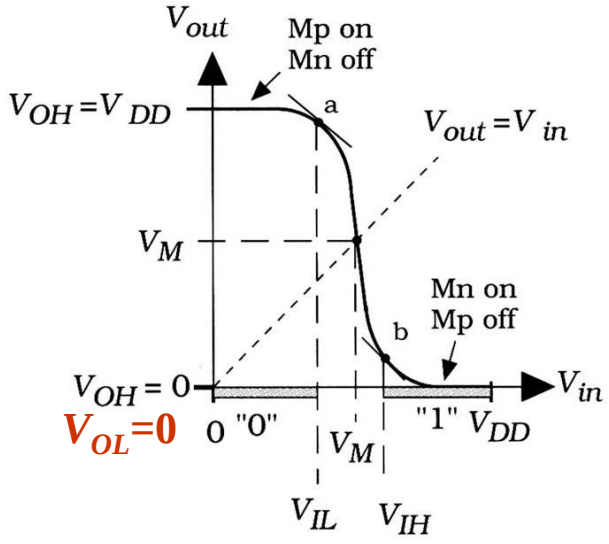
$$\frac{dV_{out}}{dV_{in}}=-1\Rightarrow V_{in}(1+\frac{\beta_n}{\beta_p})=2V_{out}-V_{DD}-|V_{Tp}|+\frac{\beta_n}{\beta_p}V_{Tn}$$

b点坐标：

$$\frac{1}{2}\beta_n[2(V_{in}-V_{Tn})V_{out}-V_{out}^2]=\frac{1}{2}\beta_p(V_{DD}-V_{in}-|V_{Tp}|)^2$$

$$\frac{dV_{out}}{dV_{in}}=-1\Rightarrow V_{in}(1+\frac{\beta_p}{\beta_n})=2V_{out}+V_{Tn}+\frac{\beta_p}{\beta_n}(V_{DD}-|V_{Tp}|)$$

2 电压传输特性曲线（VTC）



（2）噪声容限

高电平噪声容限：

$$VNM_H = V_{OH,\min} - V_{IH,\min}$$

低电平噪声容限：

$$VNM_L = V_{IL,\max} - V_{OL,\max}$$

（3）中点电压V_M

定义：VTC曲线与直线$V_{out}=V_{in}$的交点

中点电压V_M的计算：

$$\because I_{Dn} = I_{Dp}$$

$$\therefore \frac{1}{2}\beta_n (V_M - V_{Tn})^2 = \frac{1}{2}\beta_p (V_{DD} - V_M - |V_{Tp}|)^2$$

$$\therefore V_M = \frac{V_{DD} - |V_{Tp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

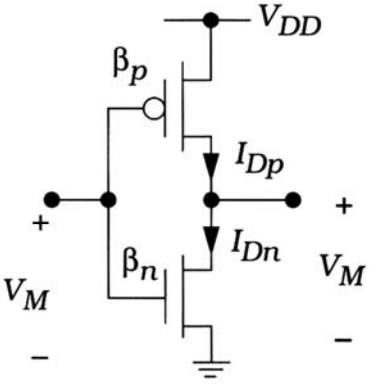


Figure 7.4 Inverter voltages for V_M calculation

§7.1 CMOS反相器的直流特性

对称反相器： $V_M = \frac{1}{2}V_{DD}$

$$\because V_M = \frac{V_{DD} - |V_{Tp}| + \sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} = \frac{1}{2}V_{DD}$$

$$\therefore \frac{\beta_n}{\beta_p} = \left(\frac{\frac{1}{2}V_{DD} - |V_{Tp}|}{\frac{1}{2}V_{DD} - V_{Tn}}\right)^2$$

若 $V_{Tn} = |V_{Tp}|$，则 $\beta_n = \beta_p$

§7.1 CMOS反相器的直流特性

例7.1 一个CMOS工艺具有下列参数：电源电压 $V_{DD} = 3.0\text{V}$

$$k_n' = 140\mu\text{A/V}^2, V_{Tn} = 0.70\text{V}, k_p' = 60\mu\text{A/V}^2, V_{Tp} = -0.70\text{V}$$

①对称设计 $\beta_n = \beta_p$

$$V_M = \frac{V_{DD} - |V_{Tp}| + \sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} = \frac{3 - 0.7 + \sqrt{1} \times 0.7}{1 + \sqrt{1}} = 1.5\text{V}$$

$$\because \frac{\beta_n}{\beta_p} = \frac{k_n'\left(\frac{W}{L}\right)_n}{k_p'\left(\frac{W}{L}\right)_p} = 1 \quad \therefore \left(\frac{W}{L}\right)_p = \frac{k_n'}{k_p'}\left(\frac{W}{L}\right)_n = \frac{140}{60}\left(\frac{W}{L}\right)_n = 2.33\left(\frac{W}{L}\right)_n$$

例7.1 一个CMOS工艺具有下列参数：电源电压 $V_{DD}=3.0\text{V}$

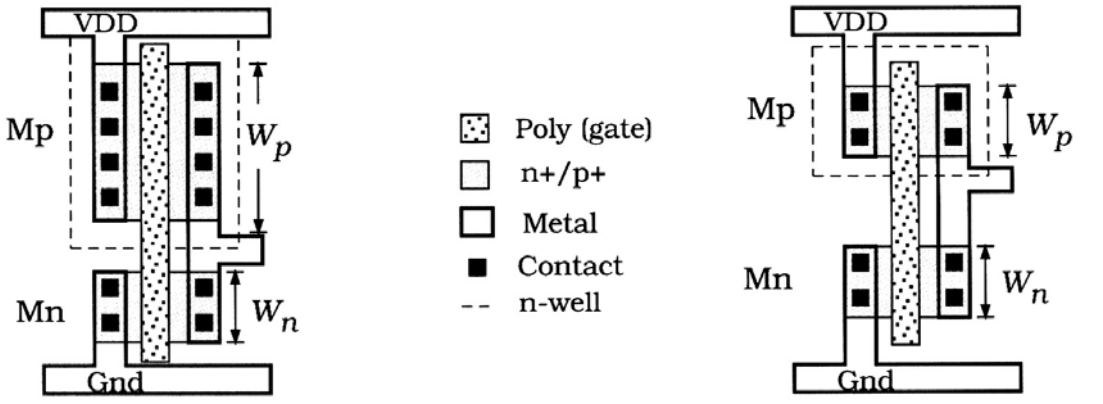
$$k_n'=140\mu\text{A/V}^2, V_{Tn}=0.70\text{V}, k_p'=60\mu\text{A/V}^2, V_{Tp}=-0.70\text{V}$$

②宽长比相等设计 $\left(\frac{W}{L}\right)_n=\left(\frac{W}{L}\right)_p$

$$\because \frac{\beta_n}{\beta_p}=\frac{k_n'\left(\frac{W}{L}\right)_n}{k_p'\left(\frac{W}{L}\right)_p}=\frac{k_n'}{k_p'}=2.33$$

$$\therefore V_M=\frac{V_{DD}-|V_{Tp}|+\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1+\sqrt{\frac{\beta_n}{\beta_p}}}=\frac{3-0.7+\sqrt{2.33}\times 0.7}{1+\sqrt{2.33}}=1.33\text{V}$$

例7.1中两种设计的版图比较



(a) Larger pFET design (b) Equal aspect ratios

Figure 7.5 Comparison of the layouts for Example 7.1

§ 7.1 CMOS反相器的直流特性

（4）中点电压V_M与器件比的关系

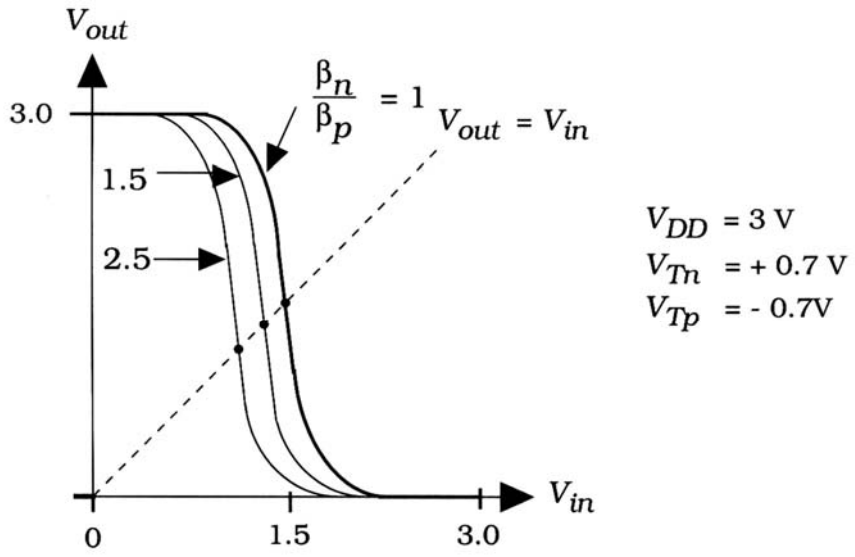


Figure 7.6 Dependence of V_M on the device ratio

§ 7.2 CMOS反相器的开关特性

反相器的开关波形

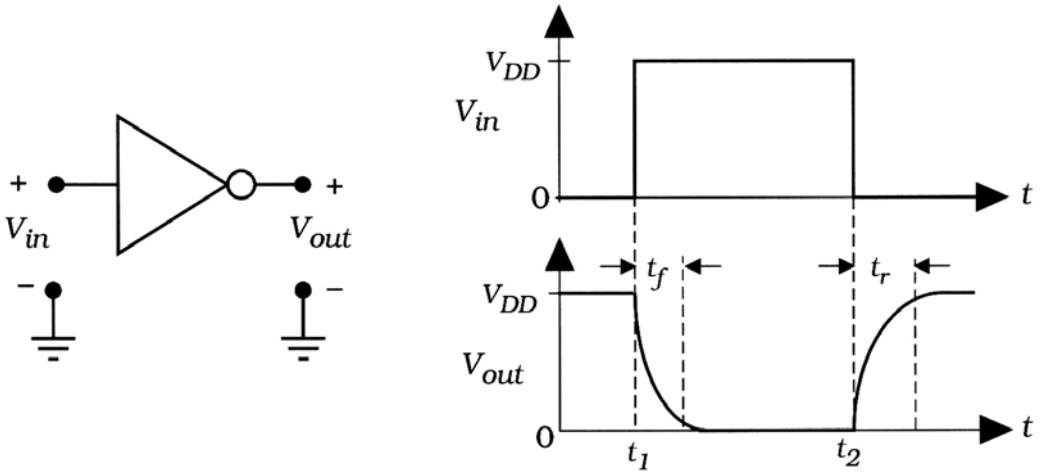
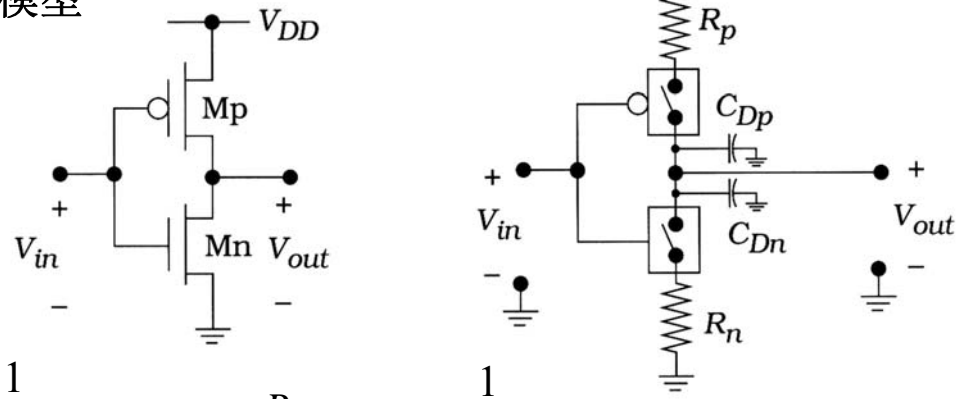


Figure 7.7 General switching waveforms

输出产生延时的原因：寄生电阻和电容。

反相器的*RC*模型

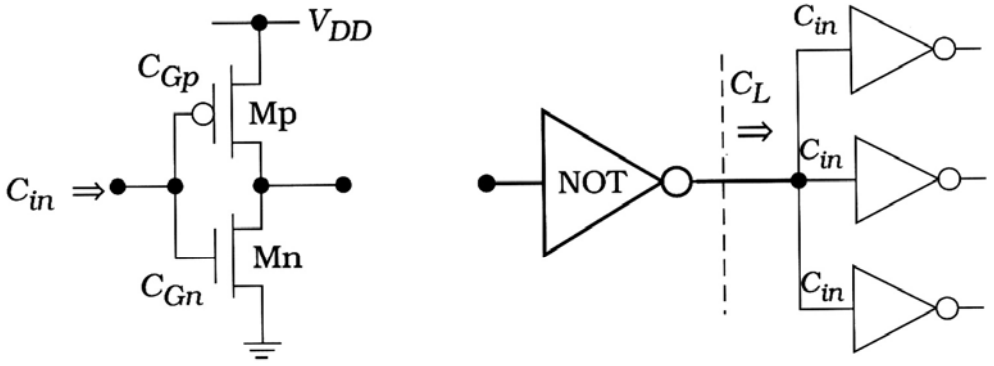


$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})} \qquad R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)}$$

$$C_{Dn} = C_{GDn} + C_{DBn} = \frac{1}{2} C_{ox} L' W_n + C_{jn} A_n + C_{jswn} P_n$$

$$C_{Dp} = C_{GDp} + C_{DBp} = \frac{1}{2} C_{ox} L' W_p + C_{jp} A_p + C_{jswp} P_p$$

输入电容与负载效应



(a) Single stage (b) Loading due to fan-out

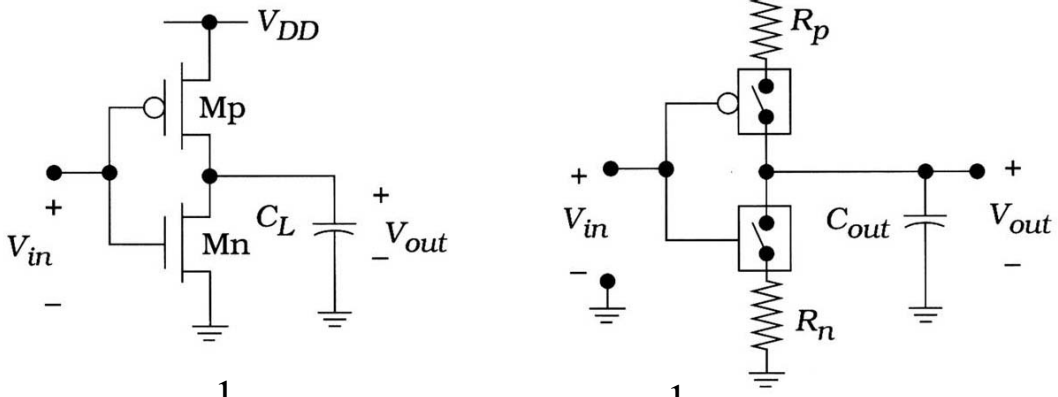
Figure 7.9 Input capacitance and load effects

扇出（***FO***）：与驱动门输出端相连的负载门的数目。

$$C_{in} = C_{Gp} + C_{Gn} \qquad C_L = FO \times C_{in} = 3C_{in}$$

§ 7.2 CMOS反相器的开关特性

完整的反相器开关模型

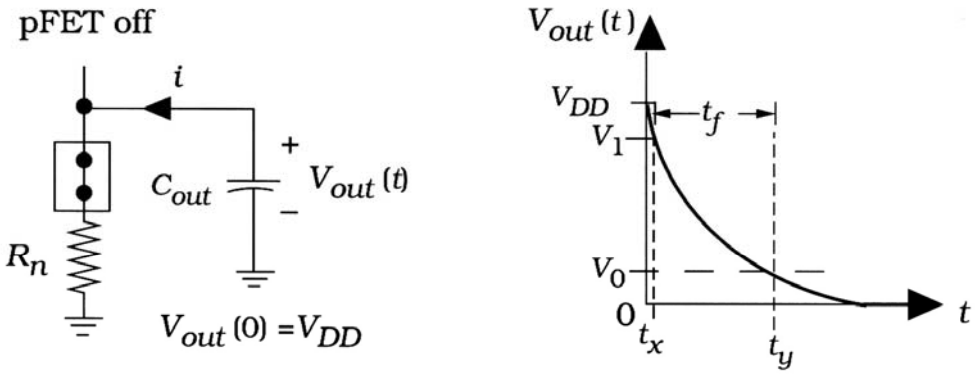


$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})} \qquad R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)}$$

$$C_{out} = C_{FET} + C_L = C_{Dn} + C_{Dp} + C_L$$

§ 7.2 CMOS反相器的开关特性

7.2.1 下降时间 t_f 计算



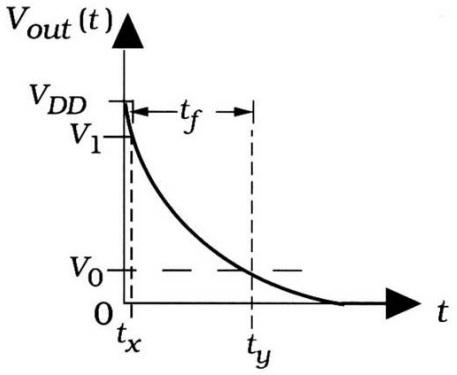
(a) Discharge circuit (b) Output waveform

Figure 7.12 Discharge circuit for the fall time calculation

$$i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{out}}{R_n} \qquad V_{out}(0) = V_{DD}$$

$$i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{out}}{R_n} \qquad V_{out}(0) = V_{DD}$$

$$\therefore V_{out}(t) = V_{DD}e^{-t/\tau_n}, \tau_n = R_nC_{out}$$



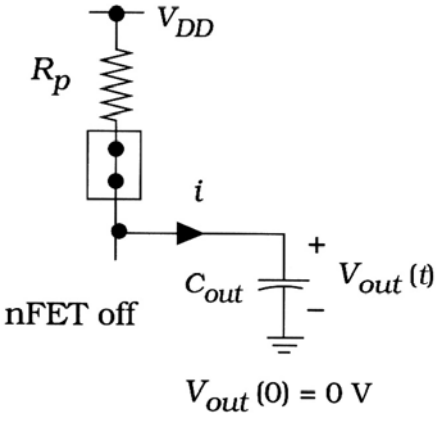
下降时间 t_f 定义：

从**0.9V_{DD}**到**0.1V_{DD}**的时间间隔。

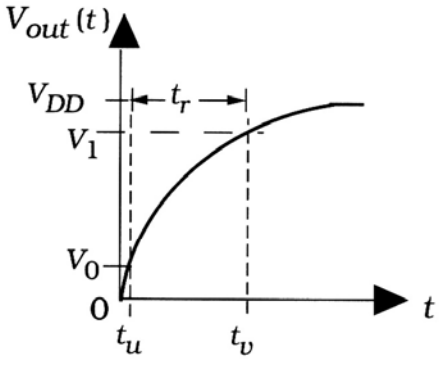
$$\ln\frac{V_{out}}{V_{DD}} = -\frac{t}{\tau_n} \qquad \therefore t = \tau_n \ln\frac{V_{DD}}{V_{out}}$$

$$\therefore t_f = t_y - t_x = \tau_n \ln 10 - \tau_n \ln\frac{10}{9} = \ln 9\tau_n \approx 2.2\tau_n = t_{HL}$$

7.2.2 上升时间 t_r 计算



(a) Charge circuit



(b) Output waveform

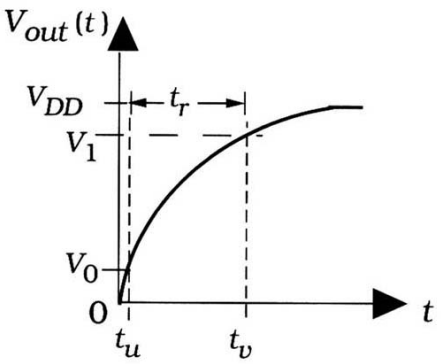
Figure 7.13 Rise time calculation

$$i = C_{out}\frac{dV_{out}}{dt} = \frac{V_{DD} - V_{out}}{R_p} \qquad V_{out}(0) = 0$$

§ 7.2 CMOS反相器的开关特性

$$i = C_{out}\frac{\mathrm{d}V_{out}}{\mathrm{d}t} = \frac{V_{DD}-V_{out}}{R_p} \qquad V_{out}(0)=0$$

$$\therefore V_{out}(t) = V_{DD}(1-e^{-t/\tau_p}),\tau_p = R_pC_{out}$$



上升时间 t_r 定义：

从$0.1V_{DD}$到$0.9V_{DD}$的时间间隔。

$$t = \tau_p \ln\frac{V_{DD}}{V_{DD}-V_{out}}$$

$$\therefore t_r = t_v - t_u = \ln 9\tau_p \approx 2.2\tau_p = t_{LH}$$

最大信号频率：$f_{\max} = \dfrac{1}{t_{HL}+t_{LH}} = \dfrac{1}{t_r+t_f}$

f_{max}是加在门上使输出仍可稳定至确定状态的最大频率。

§ 7.2 CMOS反相器的开关特性

例7.3有一个反相器电路，FET的宽长比$(W/L)_n = 6,(W/L)_p = 8$。

其工艺参数为：$k_n' = 150\mu\mathrm{A/V}^2, V_{Tn} = 0.70\mathrm{V},$

$k_p' = 62\mu\mathrm{A/V}^2, V_{Tp} = -0.85\mathrm{V}, V_{DD} = 3.3\mathrm{V}$

总输出电容估计为 $C_{out} = 150\mathrm{fF},$

求上升时间，pFET的电阻为

$$R_p = \frac{1}{\beta_p(V_{DD}-|V_{Tp}|)} = \frac{1}{62\times10^{-6}\times8\times(3.3-0.85)} = 822.9\Omega$$

充电时间常数 $\tau_p = 822.9\times150\times10^{-15} = 123.44\mathrm{ps}$

上升时间为 $t_r = 2.2\tau_p = 271.56\mathrm{ps}$

求下降时间，**nFET**的电阻为

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})} = \frac{1}{150\times10^{-6}\times6\times(3.3-0.70)} = 427.35\Omega$$

放电时间常数 $\tau_n = 427.35\times150\times10^{-15} = 64.1\text{ps}$

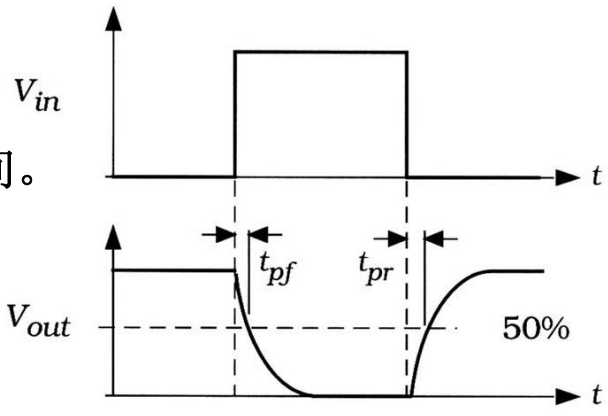
下降时间为 $t_f = 2.2\tau_n = 141.0\text{ps}$

最大信号频率为

$$f_{\max} = \frac{1}{t_r + t_f} = \frac{1}{(271.56+141.0)\times10^{-12}} = 2.42\text{GHz}$$

7.2.3 传播延时 t_p

定义：信号通过逻辑门的延时。



t_{pf}：输出从V_{DD}到$0.5V_{DD}$的下降时间。

t_{pr}：输出从0到$0.5V_{DD}$的上升时间。

$$\because t = \tau_n \ln\frac{V_{DD}}{V_{out}} \qquad \therefore t_{pf} = (\ln 2)\tau_n$$

$$\because t = \tau_p \ln\frac{V_{DD}}{V_{DD}-V_{out}} \qquad \therefore t_{pr} = (\ln 2)\tau_p$$

传播延时 t_p： $t_p = \frac{t_{pf}+t_{pr}}{2} = \frac{\ln 2}{2}(\tau_n+\tau_p) \approx 0.35(\tau_n+\tau_p)$

7.2.4 一般分析

t_r 和 t_f 的一般公式

总输出电容：$C_{out} = C_{FET} + C_L$

上升时间：$t_r = 2.2R_pC_{out} = 2.2R_p(C_{FET} + C_L) = t_{r0} + \alpha_p C_L$

其中：$t_{r0} = 2.2R_pC_{FET}$　　$\alpha_p = 2.2R_p = \dfrac{2.2}{\beta_p(V_{DD} - |V_{Tp}|)}$

下降时间：$t_f = 2.2R_nC_{out} = 2.2R_n(C_{FET} + C_L) = t_{f0} + \alpha_n C_L$

其中：$t_{f0} = 2.2R_nC_{FET}$　　$\alpha_n = 2.2R_n = \dfrac{2.2}{\beta_n(V_{DD} - V_{Tn})}$

上升时间：

$t_r = t_{r0} + \alpha_p C_L$

$t_{r0} = 2.2R_pC_{FET}$

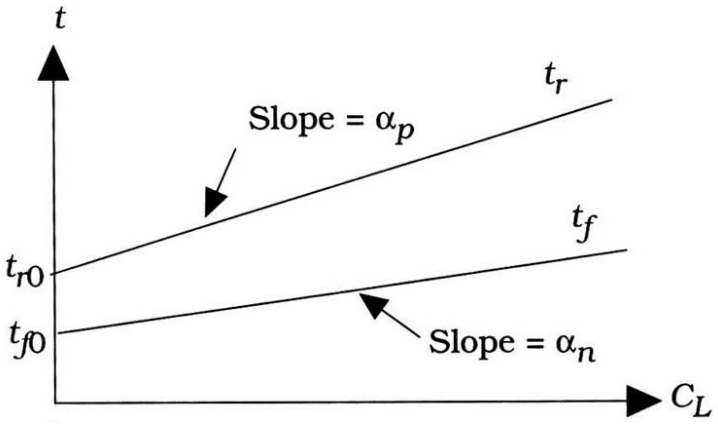
$\alpha_p = \dfrac{2.2}{\beta_p(V_{DD} - |V_{Tp}|)}$

下降时间：

$t_f = t_{f0} + \alpha_n C_L$

$t_{f0} = 2.2R_nC_{FET}$

$\alpha_n = \dfrac{2.2}{\beta_n(V_{DD} - V_{Tn})}$



快的电路比慢的电路消耗更多的面积

§ 7.2 CMOS反相器的开关特性

例7.4 利用例**7.3**的结构求**FET**内部电容为 $C_{FET}=80\text{fF}$ 情况下的一般的延时公式。

上升时间由**pFET**控制，电阻 $R_p=822.9\Omega$

斜率 $\alpha_p=2.2R_p=1810.4\Omega$

而 $t_{r0}=2.2R_pC_{FET}=2.2\times822.9\times80\times10^{-15}=144.8\text{ps}$

上升时间为 $t_r=t_{r0}+\alpha_pC_L=144.8+1.810C_L(\text{ps})$

下降时间由**nFET**控制，电阻 $R_n=427.35\Omega$

斜率 $\alpha_n=2.2R_n=940.2\Omega$

而 $t_{f0}=2.2R_nC_{FET}=2.2\times427.35\times80\times10^{-15}=75.2\text{ps}$

下降时间为 $t_f=t_{f0}+\alpha_nC_L=75.2+0.940C_L(\text{ps})$

§ 7.2 CMOS反相器的开关特性

假设负载C_L=150fF

上升时间：$t_r=144.8+1.810C_L=416.4\text{ps}$

下降时间：$t_f=75.2+0.940C_L=216.2\text{ps}$

最大信号频率为

$$f_{\max}=\frac{1}{t_r+t_f}=\frac{1}{(416.4+216.2)\times10^{-12}}=1.58\text{GHz}$$

7.2.5 反相器电路小结

一个独立的**CMOS**反相器的电气特性由两组参数确定：

1 工艺变量：例如 V_T 和 k' 值，以及寄生电容参数

2 **MOS**管的宽长比 $(W/L)_n$ 和 $(W/L)_p$

§ 7.3 功耗

$$P = V_{DD} I_{DD}$$

$$P = P_{DC} + P_{dyn}$$

P_{DC}：静态功耗

P_{dyn}：动态功耗

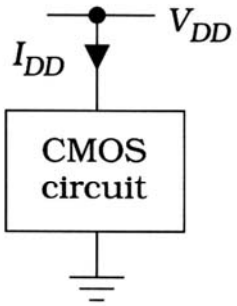


Figure 7.16 Origin of power dissipation calculation

●静态功耗：$P_{DC} = V_{DD} I_{DDQ}$　　I_{DDQ}：静态漏电流

$$I_{DDQ} = I_S + I_{sub}$$

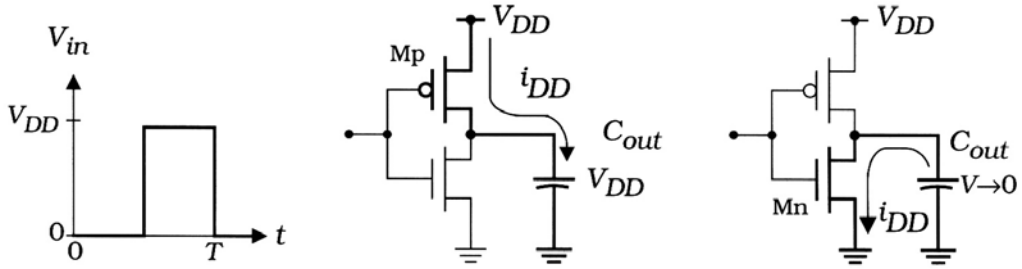
I_S：pn结反向饱和电流；I_{sub}：亚阈值电流

●动态功耗：$P_{dyn} = P_{sw} + P_{dp}$

P_{sw}：开关功耗；P_{dp}：短路功耗

§ 7.3 功耗

(1)开关功耗P_{sw}　　$P_{sw} = C_{out} V_{DD}^2 f$



(a) Input voltage　(b) Charge　(c) Discharge

Figure 7.18 Circuit for finding the transient power dissipation

(2)短路功耗P_{dp}　　$P_{dp} = \frac{\beta_n}{12}(V_{DD} - 2V_{Tn})^3 \times \frac{t_r}{0.8} \times f$

总功耗：$P = V_{DD} I_{DDQ} + C_{out} V_{DD}^2 f + \frac{\beta_n}{12}(V_{DD} - 2V_{Tn})^3 \times \frac{t_r}{0.8} \times f$

§ 7.4 DC特性：与非门和或非门

7.4.1 与非门（NAND）分析

与非门的直流特性

设同极性FET具有同样*W/L*

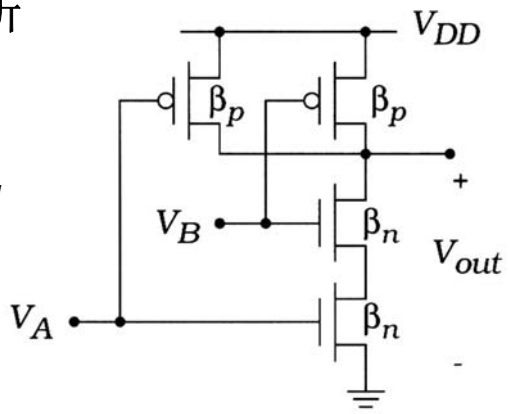


Figure 7.19 NAND2 logic circuit

互补CMOS逻辑门的优点：

（1）$V_{OH,max}=V_{DD}$，$V_{OL,min}=0$；逻辑摆幅：$V_L=V_{DD}$。

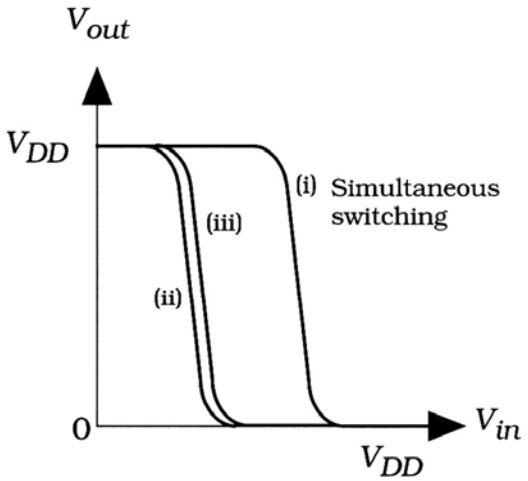
（2）电路的静态功耗极小。

§ 7.4 DC特性：与非门和或非门

二输入与非门的电压传输特性曲线

	V_A	V_B	V_{out}
(i)	0	0	V_{DD}
(ii)	0	V_{DD}	V_{DD}
(iii)	V_{DD}	0	V_{DD}
	V_{DD}	V_{DD}	0

(a) Transition table



(b) VTC family

Figure 7.20 NAND2 VTC analysis

§ 7.4 DC特性：与非门和或非门

用于V_M计算的NAND2版图

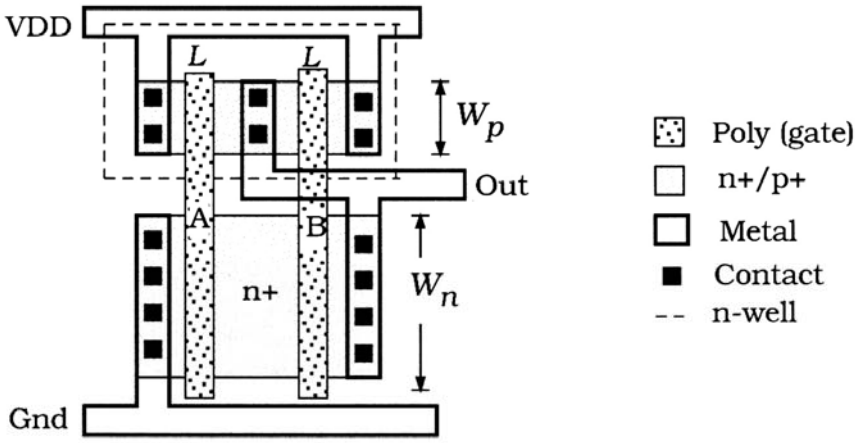
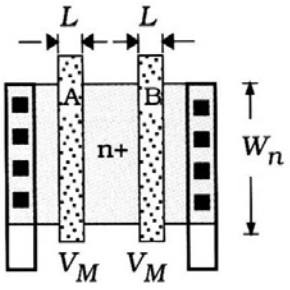


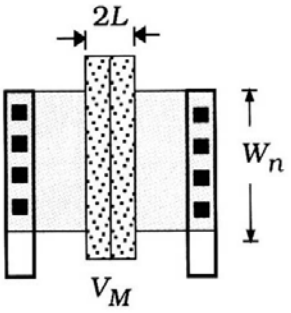
Figure 7.21 Layout of NAND2 for V_M calculation

§ 7.4 DC特性：与非门和或非门

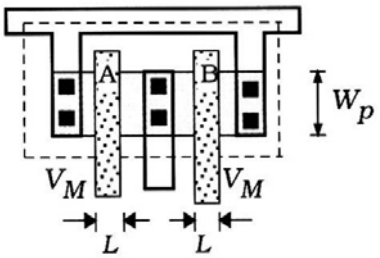
同时切换下的中点电压

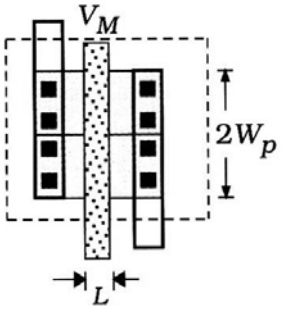
串联nFET的简化



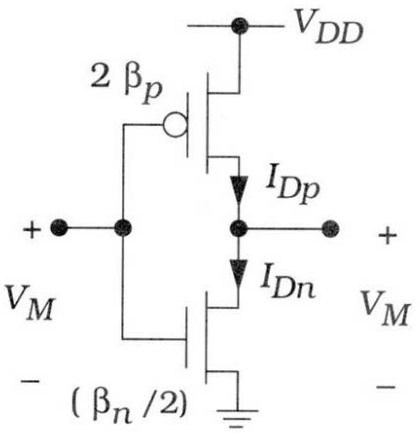


并联pFET的简化





NAND2门求中点电压的简化电路



$$\frac{(\beta_n/2)}{2}(V_M - V_{Tn})^2 = \frac{(2\beta_p)}{2}\left(V_{DD} - V_M - |V_{Tp}|\right)^2$$

$$V_M = \frac{V_{DD} - |V_{Tp}| + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}}$$

N输入与非门的中点电压： $V_M = \dfrac{V_{DD} - |V_{Tp}| + \frac{1}{N}\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + \frac{1}{N}\sqrt{\frac{\beta_n}{\beta_p}}}$

7.4.2 或非门（NOR）分析

或非门的直流特性

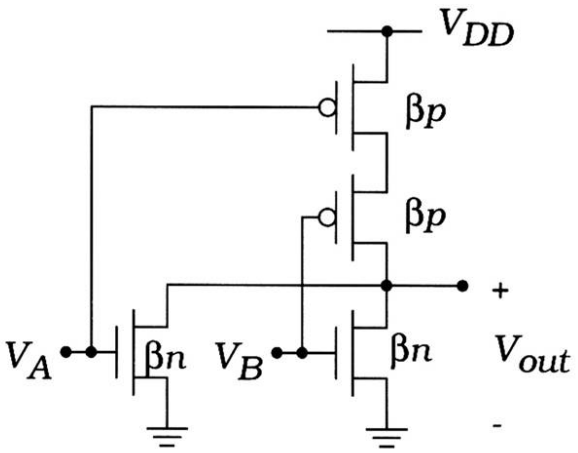


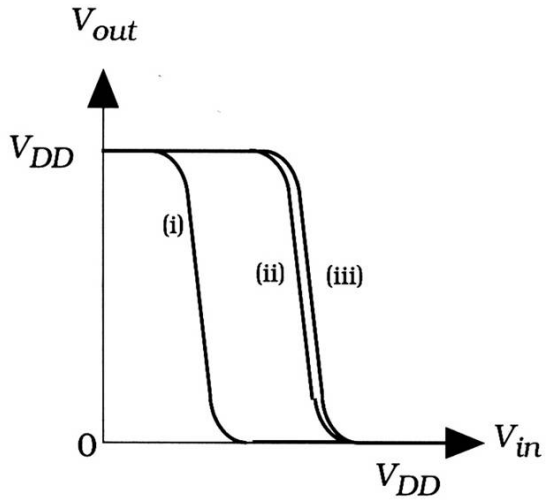
Figure 7.25 NOR2 circuit

§ 7.4 DC特性：与非门和或非门

二输入或非门的电压传输特性曲线

	V_A	V_B	V_{out}
	0	0	V_{DD}
(iii)	0	V_{DD}	0
(ii)	V_{DD}	0	0
(i)	V_{DD}	V_{DD}	0

(a) Transition table

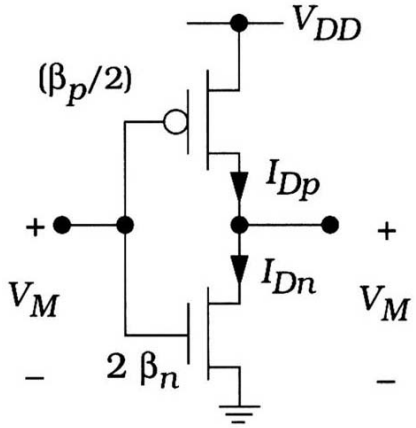


(b) VTC family

Figure 7.26 NOR2 VTC construction

§ 7.4 DC特性：与非门和或非门

NOR2门求中点电压的简化电路



$$\frac{(2\beta_n)}{2}(V_M - V_{Tn})^2 = \frac{(\beta_p/2)}{2}\left(V_{DD} - V_M - |V_{Tp}|\right)^2$$

$$V_M = \frac{V_{DD} - |V_{Tp}| + 2\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + 2\sqrt{\frac{\beta_n}{\beta_p}}}$$

N输入或非门的中点电压： $$V_M = \frac{V_{DD} - |V_{Tp}| + N\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + N\sqrt{\frac{\beta_n}{\beta_p}}}$$

7.5.1 NAND2门开关时间

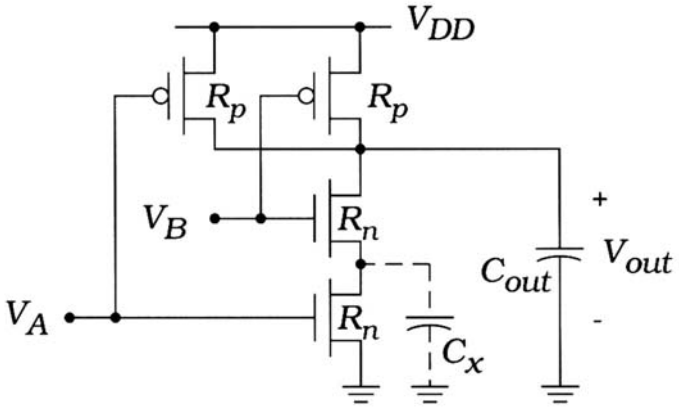
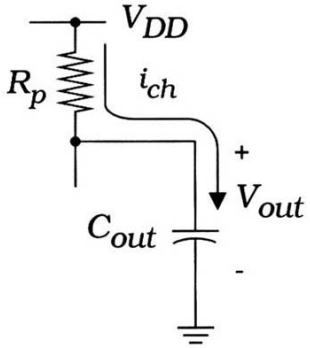


Figure 7.28 NAND2 circuit for transient calculations

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})} \qquad R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)}$$

$$C_{out} = C_{FET} + C_L \qquad C_{FET} = C_{Dn} + 2C_{Dp}$$



(a) Charging circuit

上升时间t_r

$$V_{out}(t) = V_{DD}(1 - e^{-t/\tau_p})$$

$$\tau_p = R_p C_{out}$$

$$t_r = 2.2\tau_p = 2.2R_p(C_{FET} + C_L)$$
$$= 2.2R_p C_{FET} + 2.2R_p C_L$$
$$= t_0 + \alpha_0 C_L$$

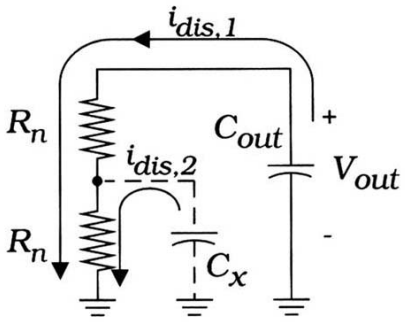
t_0：零负载延时；

α_0：t_r作为负载电容C_L函数的斜率。

下降时间t_f

$$V_{out}(t) = V_{DD}e^{-t/\tau_n}$$

$$\tau_n = 2R_nC_{out} + R_nC_x$$



(b) Discharging circuit

CMOS电路中，串联MOS管会导致较长延时。

$$t_f = 2.2\tau_n$$
$$= 2.2[2R_n(C_{FET} + C_L) + R_nC_x]$$
$$= 2.2[R_n(2C_{FET} + C_x) + 2R_nC_L]$$
$$= t_1 + \alpha_1 C_L$$

其中：$t_1 = 2.2R_n(2C_{FET} + C_x)$

$$\alpha_1 = 4.4R_n$$

7.5.2 NOR2门开关时间

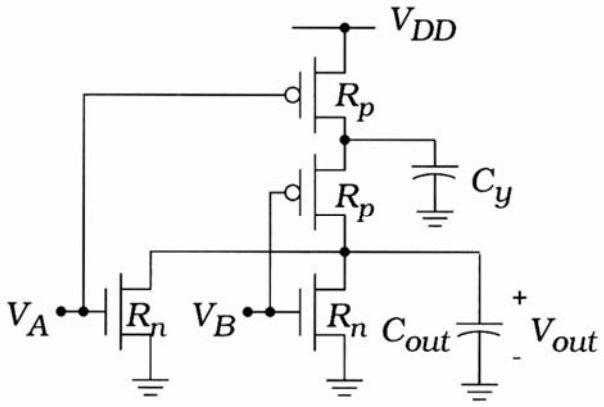
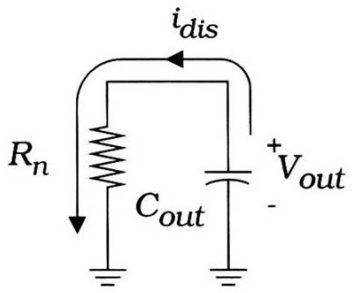


Figure 7.30 NOR2 circuit for switching time calculations

$$R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})} \qquad R_p = \frac{1}{\beta_p(V_{DD} - |V_{Tp}|)}$$

$$C_{out} = C_{FET} + C_L \qquad C_{FET} = 2C_{Dn} + C_{Dp}$$

下降时间t_f



(a) Discharging circuit

$$V_{out}(t) = V_{DD}e^{-t/\tau_n}$$

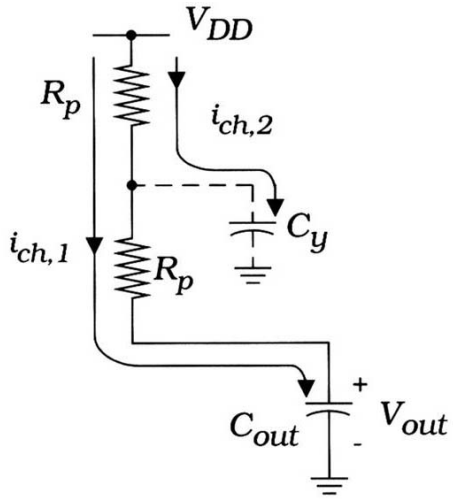
$$\tau_n = R_n C_{out}$$

$$t_f = 2.2\tau_n = 2.2R_n(C_{FET} + C_L)$$
$$= 2.2R_n C_{FET} + 2.2R_n C_L$$
$$= t_1 + \alpha_1 C_L$$

t_1：零负载延时；

α_1：t_f作为负载电容C_L函数的斜率。

上升时间t_r



(b) Charging circuit

$$V_{out}(t) = V_{DD}(1 - e^{-t/\tau_p})$$

$$\tau_p = 2R_p C_{out} + R_p C_y$$

$$t_r = 2.2\tau_p$$
$$= 2.2[2R_p(C_{FET} + C_L) + R_p C_y]$$
$$= 2.2[R_p(2C_{FET} + C_y) + 2R_p C_L]$$
$$= t_0 + \alpha_0 C_L$$

其中：$t_0 = 2.2R_p(2C_{FET} + C_y)$

$$\alpha_0 = 4.4R_p$$

§ 7.5 与非门和或非门的暂态响应

7.5.3 小结

上升时间t_r：　$t_r = t_0 + \alpha_0 C_L$

下降时间t_f：　$t_f = t_1 + \alpha_1 C_L$

$t_0, \alpha_0, t_1, \alpha_1$ 取决于晶体管的寄生电阻和寄生电容；

开关延时随扇入的增加而增加；

开关延时随外加负载的增加而增加；

逻辑门的电气特性由几组参数确定：

① 工艺变量

② MOS管的宽长比 $(W/L)_n$ 和 $(W/L)_p$

③ 版图几何图的细节影响逻辑门的暂态响应

§ 7.6 复合逻辑门的分析

1 开关时间

上升时间t_r：

$t_r = t_0 + \alpha_0 C_L$

$t_0 = 2.2R_p(C_p + 2C_{FET})$

$\alpha_0 = 4.4R_p$

下降时间t_f：

$t_f = t_1 + \alpha_1 C_L$

$t_1 = 2.2R_n(C_n + 2C_{FET})$

$\alpha_1 = 4.4R_n$

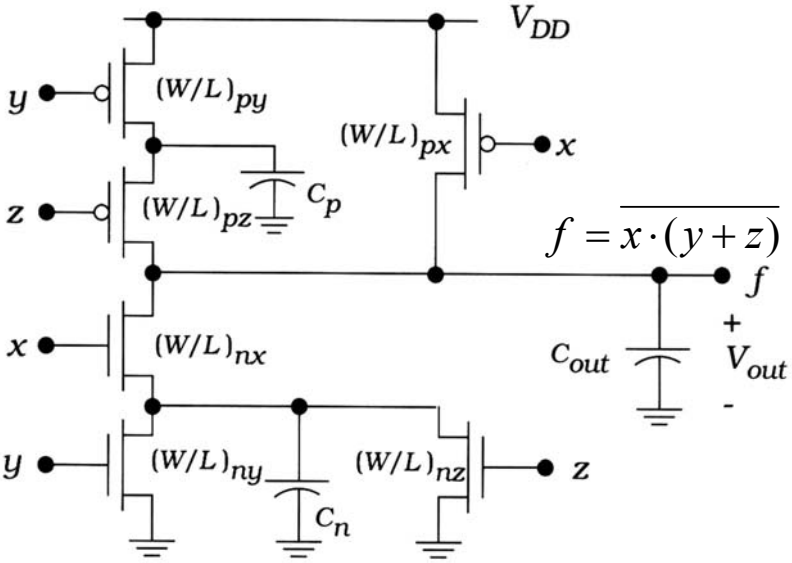


Figure 7.32 Complex logic gate circuit

2 功耗

反相器功耗： $P = P_{DC} + P_{dp} + P_{sw}$ $\qquad P_{sw} = C_{out} V_{DD}^2 f$

一般的静态CMOS逻辑门：

开关功耗： $P_{sw} = aC_{out} V_{DD}^2 f$

翻转系数a：在一个周期内发生一次输出**0→1**转换的概率。

N个门组成的电路： $P_{sw} = \sum_{i=1}^{N} a_i C_i V_i V_{DD} f$

a_i：第 i 个门的翻转系数；

C_i：充电到最大值 V_i 的节点电容。

由真值表确定翻转系数

A	B	$\overline{A+B}$	$\overline{A \cdot B}$
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	0

Figure 7.33 Truth tables for determining activity coefficients

$a = p_0 p_1$ $\qquad$ p_0：输出初始为**0**的概率

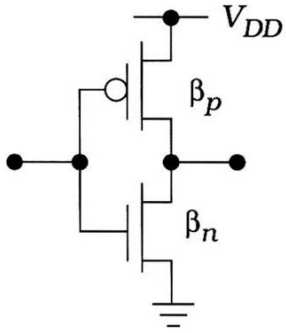
p_1：输出转变为**1**的概率

$$a_{\mathrm{NOR2}} = \frac{3}{4} \times \frac{1}{4} = \frac{3}{16} \qquad a_{\mathrm{NAND2}} = \frac{1}{4} \times \frac{3}{4} = \frac{3}{16}$$

$$a_{\mathrm{NOR3}} = \frac{7}{8} \times \frac{1}{8} = \frac{7}{64} = a_{\mathrm{NAND3}} \qquad a_{\mathrm{XNOR2}} = \frac{1}{2} \times \frac{1}{2} = \frac{1}{4} = a_{\mathrm{XOR2}}$$

§ 7.7 逻辑门过渡特性设计

1 参照门的设计



(a) Inverter

（1） 对称设计 $t_r = t_f$

$$t_r = 2.2R_pC_{out} \qquad t_f = 2.2R_nC_{out}$$

$$R_p = \frac{1}{\beta_p(V_{DD} - |V_{Tp}|)} \qquad R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})}$$

$$\beta_p = \beta_n \qquad \beta_p = k_p'\left(\frac{W}{L}\right)_p \qquad \beta_n = k_n'\left(\frac{W}{L}\right)_n$$

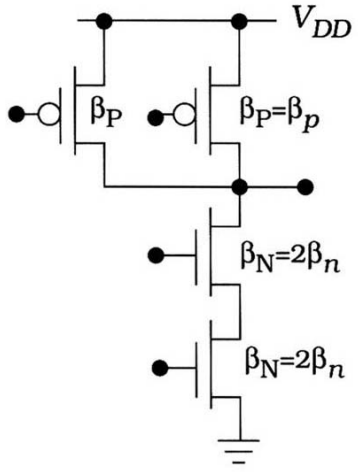
$$\therefore \left(\frac{W}{L}\right)_p = \frac{k_n'}{k_p'}\left(\frac{W}{L}\right)_n = r\left(\frac{W}{L}\right)_n$$

（2） 使用面积相同的NMOS和PMOS设计参照门

$$\left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n \Rightarrow R_p = rR_n \Rightarrow t_r = rt_f$$

§ 7.7 逻辑门过渡特性设计

2 NAND2门的设计



(b) NAND2

并联PMOS： $\beta_P = \beta_p$

串联NMOS： $2R_N = R_n$

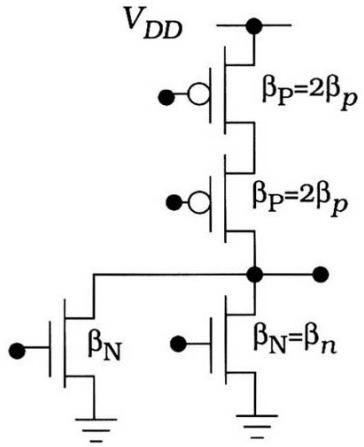
$$\frac{2}{\beta_N(V_{DD} - V_{Tn})} = \frac{1}{\beta_n(V_{DD} - V_{Tn})}$$

$$\therefore \beta_N = 2\beta_n, \left(\frac{W}{L}\right)_N = 2\left(\frac{W}{L}\right)_n$$

*N*输入与非门： $\beta_P = \beta_p \qquad \beta_N = N\beta_n$

$$\left(\frac{W}{L}\right)_P = \left(\frac{W}{L}\right)_p \qquad \left(\frac{W}{L}\right)_N = N\left(\frac{W}{L}\right)_n$$

3 NOR2门的设计



(c) NOR2

并联NMOS： $\beta_N = \beta_n$

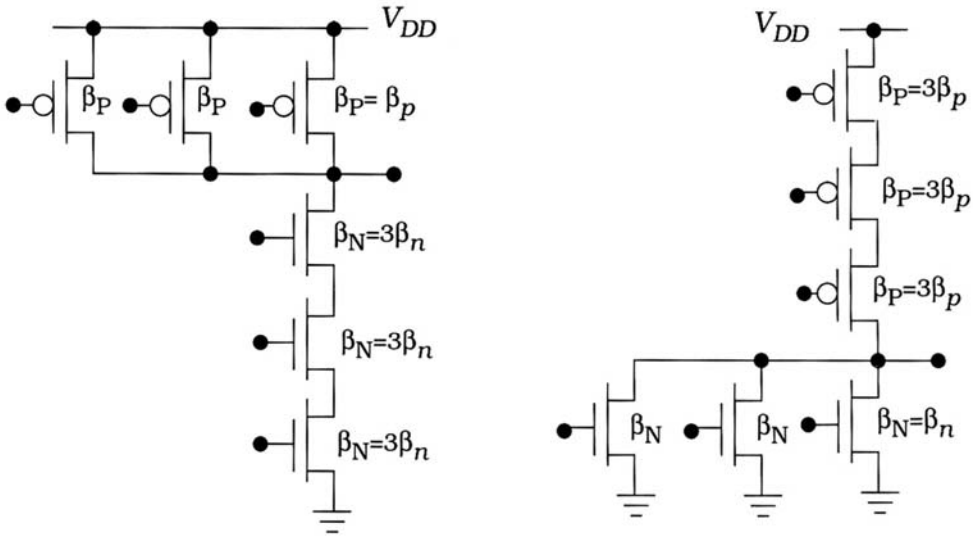
串联PMOS： $\beta_P = 2\beta_p$

*N*输入或非门：

$$\beta_N = \beta_n \qquad \beta_P = N\beta_p$$

$$\left(\frac{W}{L}\right)_N = \left(\frac{W}{L}\right)_n \qquad \left(\frac{W}{L}\right)_P = N\left(\frac{W}{L}\right)_p$$

4 NAND3门和NOR3门的设计



(a) NAND3 (b) NOR3

Figure 7.35 Sizing for 3-input gates

§ 7.7 逻辑门过渡特性设计

5 复合逻辑门的设计

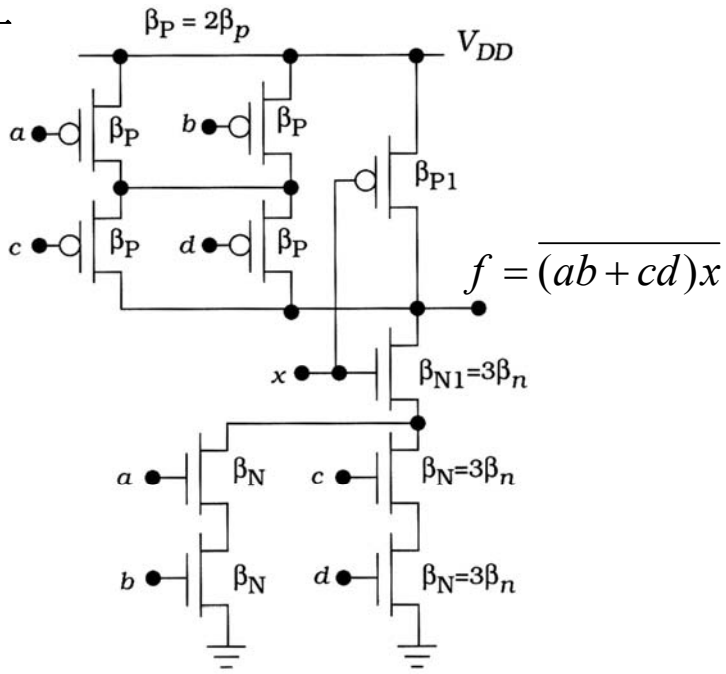
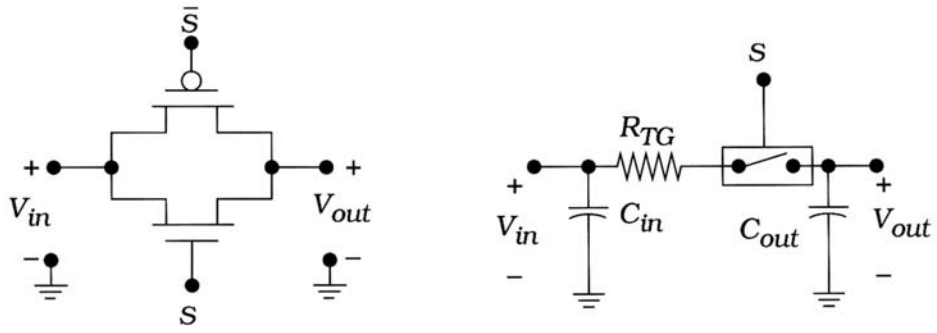


Figure 7.36 Sizing of a complex logic gate

§ 7.8 传输门和传输管

1 传输门



(a) Circuit (b) RC model

Figure 7.37 Transmission gate modeling

***RC*模型：假设输入电压比输出电压高**

$$C_{in} = C_{D,n} + C_{S,p} = C_{GDn} + C_{DBn} + C_{GSp} + C_{SBp}$$

$$C_{out} = C_{S,n} + C_{D,p} + C_L = C_{GSn} + C_{SBn} + C_{GDp} + C_{DBp} + C_L$$

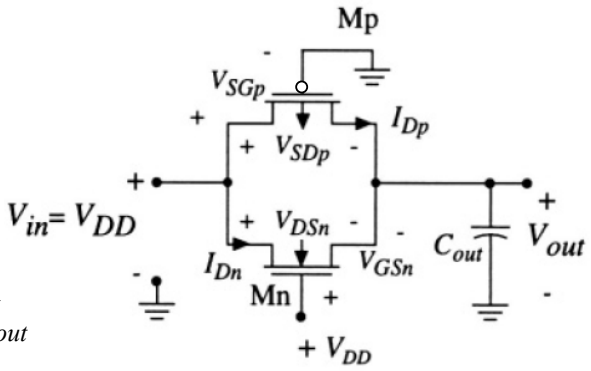
$$R_{TG} = \max(R_n, R_p) \ ? \qquad R_{TG} = R_n // R_p$$

§ 7.8 传输门和传输管

传输门电阻

$$R_n = \frac{V_{DSn}}{I_{Dn}}, R_p = \frac{V_{SDp}}{I_{Dp}}, R_{TG} = R_n // R_p$$

$$V_{in} = V_{DD}, V_{out}(0) = 0$$



NMOS：

$$V_{GSn} = V_{DD} - V_{out}, V_{DSn} = V_{DD} - V_{out}$$

(1)$V_{out} < V_{DD} - V_{Tn}$ 饱和状态

$$I_{Dn} = \frac{\beta_n}{2}(V_{GSn} - V_{Tn})^2$$

$$R_n = \frac{V_{DSn}}{I_{Dn}} = \frac{2V_{DSn}}{\beta_n(V_{GSn} - V_{Tn})^2} = \frac{2(V_{DD} - V_{out})}{\beta_n(V_{DD} - V_{out} - V_{Tn})^2}$$

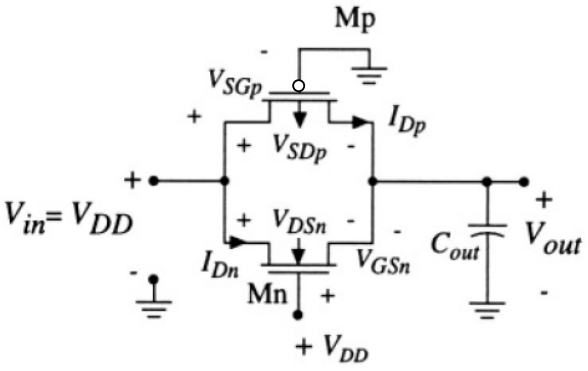
(2)$V_{out} \geq V_{DD} - V_{Tn}$ 截止状态 $R_n \to \infty$

§ 7.8 传输门和传输管

传输门电阻

$$R_n = \frac{V_{DSn}}{I_{Dn}}, R_p = \frac{V_{SDp}}{I_{Dp}}, R_{TG} = R_n // R_p$$

$$V_{in} = V_{DD}, V_{out}(0) = 0$$



PMOS：

$$V_{SGp} = V_{DD}, V_{SDp} = V_{DD} - V_{out}$$

(1)$V_{out} < |V_{Tp}|$ 饱和状态

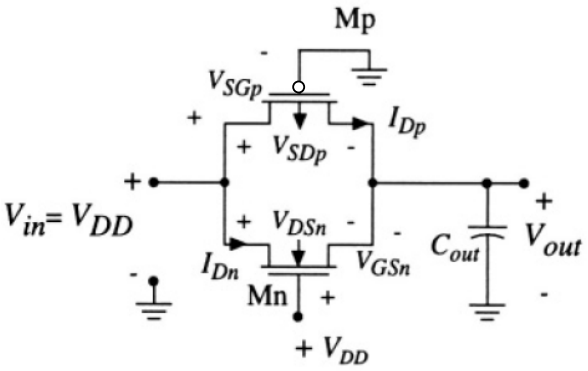
$$I_{Dp} = \frac{\beta_p}{2}(V_{SGp} - |V_{Tp}|)^2$$

$$R_p = \frac{V_{SDp}}{I_{Dp}} = \frac{2V_{SDp}}{\beta_p(V_{SGp} - |V_{Tp}|)^2} = \frac{2(V_{DD} - V_{out})}{\beta_p(V_{DD} - |V_{Tp}|)^2}$$

传输门电阻

$$R_n = \frac{V_{DSn}}{I_{Dn}}, R_p = \frac{V_{SDp}}{I_{Dp}}, R_{TG} = R_n // R_p$$

$$V_{in} = V_{DD}, V_{out}(0) = 0$$



PMOS：

$$V_{SGp} = V_{DD}, V_{SDp} = V_{DD} - V_{out}$$

$(2) V_{out} \geq |V_{Tp}|$ 非饱和状态

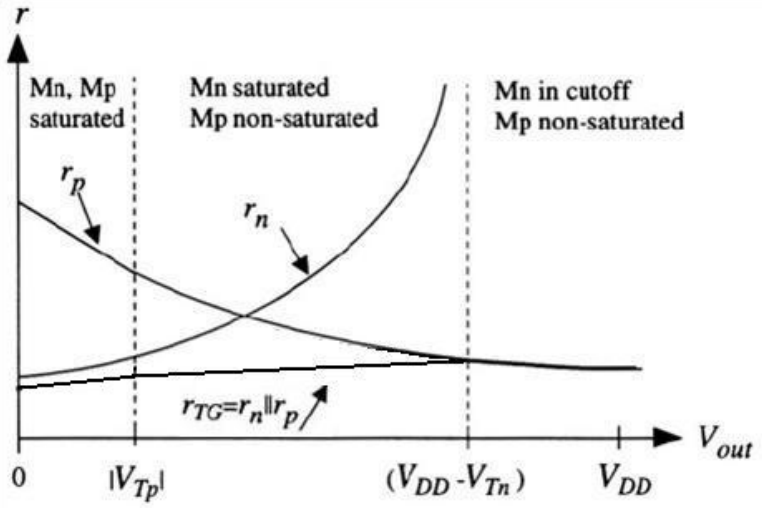
$$I_{Dp} = \frac{\beta_p}{2}[2(V_{SGp} - |V_{Tp}|)V_{SDp} - V_{SDp}^2]$$

$$R_p = \frac{V_{SDp}}{I_{Dp}} = \frac{2V_{SDp}}{\beta_p[2(V_{SGp} - |V_{Tp}|)V_{SDp} - V_{SDp}^2]} = \frac{2}{\beta_p[2(V_{DD} - |V_{Tp}|) - V_{DD} + V_{out}]}$$

$V_{out} < |V_{Tp}|$ **NMOS，PMOS均饱和**

$|V_{Tp}| \leq V_{out} < V_{DD} - V_{Tn}$ **NMOS饱和，PMOS非饱和**

$V_{out} \geq V_{DD} - V_{Tn}$ **NMOS截止，PMOS非饱和**



近似分析：选择V_{out}=0，NMOS、PMOS均饱和

$$R_n = \frac{V_{DSn}}{I_{Dn}} = \frac{2(V_{DD} - V_{out})}{\beta_n (V_{DD} - V_{out} - V_{Tn})^2} = \frac{2V_{DD}}{\beta_n (V_{DD} - V_{Tn})^2}$$

$$R_p = \frac{V_{SDp}}{I_{Dp}} = \frac{2(V_{DD} - V_{out})}{\beta_p (V_{DD} - |V_{Tp}|)^2} = \frac{2V_{DD}}{\beta_p (V_{DD} - |V_{Tp}|)^2}$$

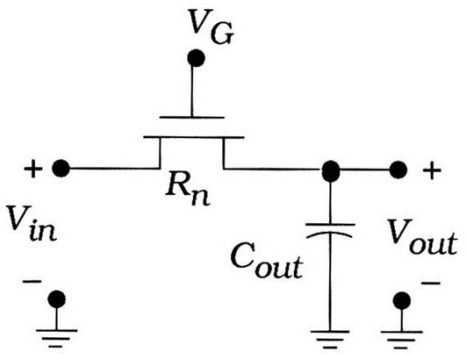
$$R_{TG} = R_n // R_p$$

若V_{Tn}=|V_{Tp}|=V_T

$$R_{TG} = R_n // R_p = \frac{2V_{DD}}{(\beta_n + \beta_p)(V_{DD} - V_T)^2}$$

2 传输管

（1）传送逻辑1



$$V_G = V_{DD}, V_{in} = V_{DD}, V_{out}(0) = 0$$

$$V_{GSn} = V_{DD} - V_{out}, V_{DSn} = V_{DD} - V_{out} = V_{GSn}$$

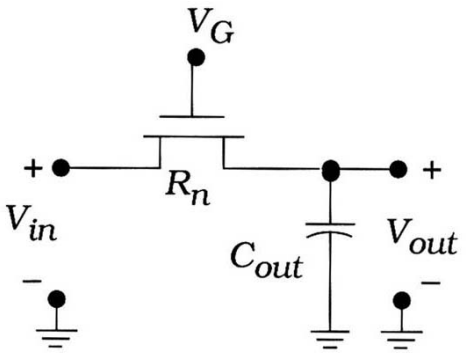
$$I_{Dn} = \frac{\beta_n}{2}(V_{GSn} - V_{Tn})^2$$

$$= \frac{\beta_n}{2}(V_{DD} - V_{out} - V_{Tn})^2 = C_{out}\frac{dV_{out}}{dt}$$

$$\therefore V_{out}(t) = (V_{DD} - V_{Tn})\frac{t/2\tau_n}{1 + t/2\tau_n}$$

$$\tau_n = R_n C_{out} = \frac{C_{out}}{\beta_n (V_{DD} - V_{Tn})}$$

（1）传送逻辑1



$$V_{out}(t)=(V_{DD}-V_{Tn})\frac{t/2\tau_n}{1+t/2\tau_n}$$

$$\because \lim_{t\to\infty}V_{out}(t)=V_{DD}-V_{Tn}=V_{\max}$$

$$\therefore V_{out}(t)=V_{\max}\frac{t/2\tau_n}{1+t/2\tau_n}$$

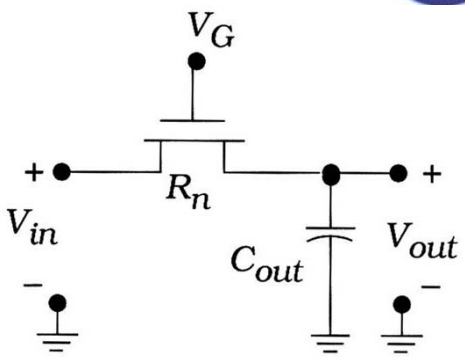
上升时间t_r：

输出电压从**0V→0.9V_{max}**的时间

$$0.9V_{\max}=V_{\max}\frac{t_r/2\tau_n}{1+t_r/2\tau_n}$$

$$\therefore t_r=18\tau_n$$

（1）传送逻辑1



考虑体效应

$$V_{Tn}=V_{T0n}+\gamma(\sqrt{2|\phi_F|+V_{out}}-\sqrt{2|\phi_F|})$$

$$V_{\max}=V_{DD}-V_{Tn}=V_{DD}-V_{T0n}-\gamma(\sqrt{2|\phi_F|+V_{\max}}-\sqrt{2|\phi_F|})$$

若 $V_{DD}=3.3\text{V},V_{T0n}=0.7\text{V},2|\phi_F|=0.58\text{V},\gamma=0.08\text{V}^{\frac{1}{2}}$

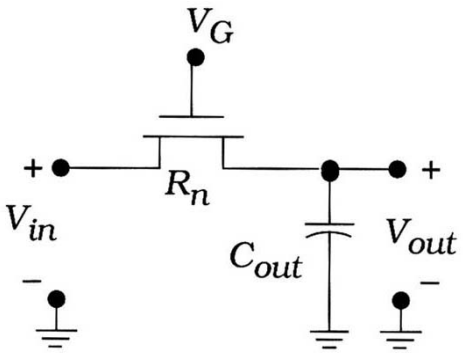
$$V_{\max}=3.3-0.7-0.08(\sqrt{0.58+V_{\max}}-\sqrt{0.58})$$

$$V_{\max}\approx 2.52\text{V}$$

（2）传送逻辑0

$$V_G = V_{DD}, V_{in} = 0, V_{out}(0) = V_{\max}$$

$$V_{GSn} = V_{DD}, V_{DSn} = V_{out} \le V_{DD} - V_{Tn} = V_{GSn} - V_{Tn}$$



$$I_{Dn} = \frac{\beta_n}{2}[2(V_{GSn} - V_{Tn})V_{DSn} - V_{DSn}^2]$$

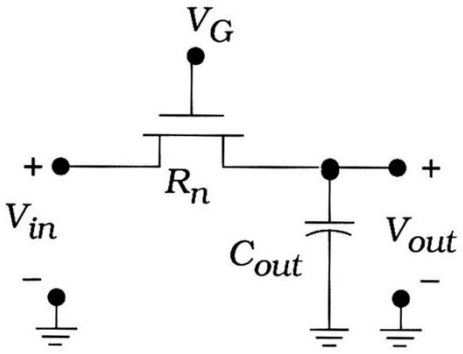
$$= \frac{\beta_n}{2}[2(V_{DD} - V_{Tn})V_{out} - V_{out}^2] = -C_{out}\frac{\mathrm{d}V_{out}}{\mathrm{d}t}$$

$$\therefore V_{out}(t) = V_{\max}\frac{2e^{-t/\tau_n}}{1+e^{-t/\tau_n}}$$

$$\tau_n = R_n C_{out}$$

（2）传送逻辑0

$$V_{out}(t) = V_{\max}\frac{2e^{-t/\tau_n}}{1+e^{-t/\tau_n}}$$



下降时间t_f:

输出电压从$V_{\max}$ →$0.1V_{\max}$的时间

$$0.1V_{\max} = V_{\max}\frac{2e^{-t_f/\tau_n}}{1+e^{-t_f/\tau_n}}$$

$$t_f \approx 2.94\tau_n$$

$$\therefore t_r \approx 6t_f$$

NMOS传输管的电压波形

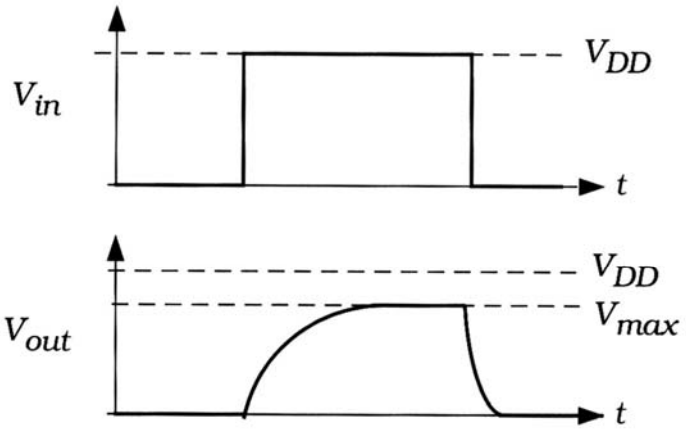


Figure 7.39 Voltage waveforms for a nFET pass transistor

PMOS管

（1）传送逻辑0

$$V_{out}(t)=|V_{Tp}|+\frac{V_{DD}-|V_{Tp}|}{1+t/2\tau_p} \qquad \tau_p=R_pC_{out}$$

下降时间t_f：输出电压从$V_{DD}\rightarrow|V_{Tp}|+0.1(V_{DD}-|V_{Tp}|)$的时间

$$t_f=18\tau_p$$

（2）传送逻辑1

$$V_{out}(t)=V_{DD}-(V_{DD}-|V_{Tp}|)\frac{2e^{-t/\tau_p}}{1+e^{-t/\tau_p}} \qquad \tau_p=R_pC_{out}$$

上升时间t_r：输出电压从$|V_{Tp}|\rightarrow|V_{Tp}|+0.9(V_{DD}-|V_{Tp}|)$的时间

$$t_r=\ln 19\tau_p\approx 2.94\tau_p$$