

第 12 章 CMOS VLSI 运算电路

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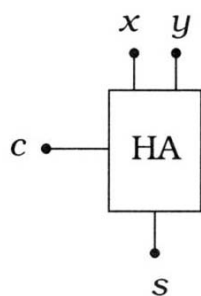
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§ 12.1 一位加法器电路

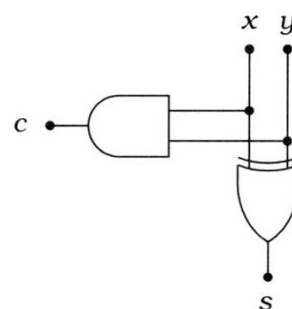
1 半加器的符号及真值表



x	y	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

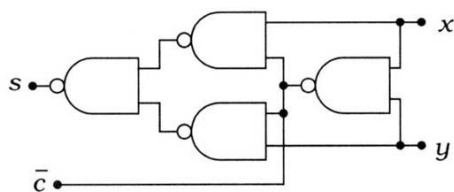
$$s = x \oplus y$$

$$c = x \cdot y$$

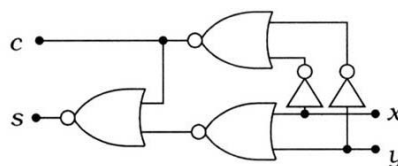


半加器的逻辑电路

另外两种半加器的逻辑电路



(a) NAND2 logic



(b) NOR-based network

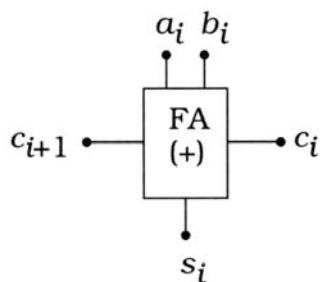
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§ 12.1 一位加法器电路

2 全加器的符号及真值表



a_i	b_i	c_i	s_i	c_{i+1}
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Figure 12.4 Full-adder symbol and function table

$$c_{i+1} = a_i \cdot b_i + c_i \cdot (a_i \oplus b_i)$$

$$= a_i \cdot b_i + c_i \cdot (a_i + b_i)$$

$$s_i = a_i \oplus b_i \oplus c_i$$

$$= a_i b_i c_i + \bar{c}_{i+1} (a_i + b_i + c_i)$$

§ 12.1 一位加法器电路

(1) AOI实现的全加器逻辑电路

$$c_{i+1} = a_i \cdot b_i + c_i \cdot (a_i + b_i)$$

$$s_i = a_i \cdot b_i \cdot c_i + \bar{c}_{i+1} \cdot (a_i + b_i + c_i)$$

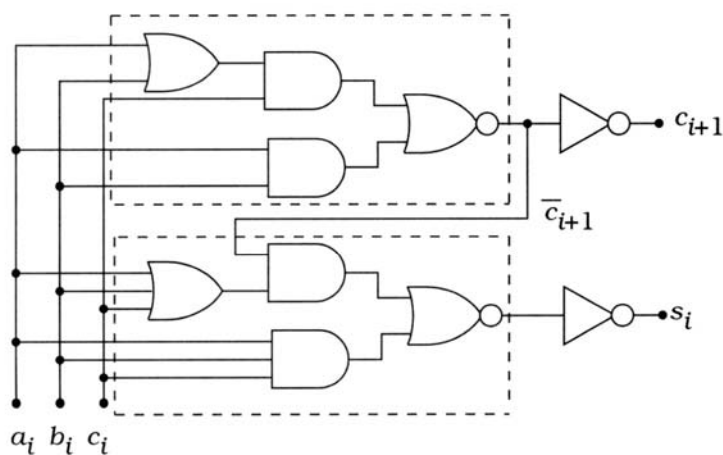


Figure 12.7 AOI full-adder logic

§ 12.1 一位加法器电路



进位输出电路的改进

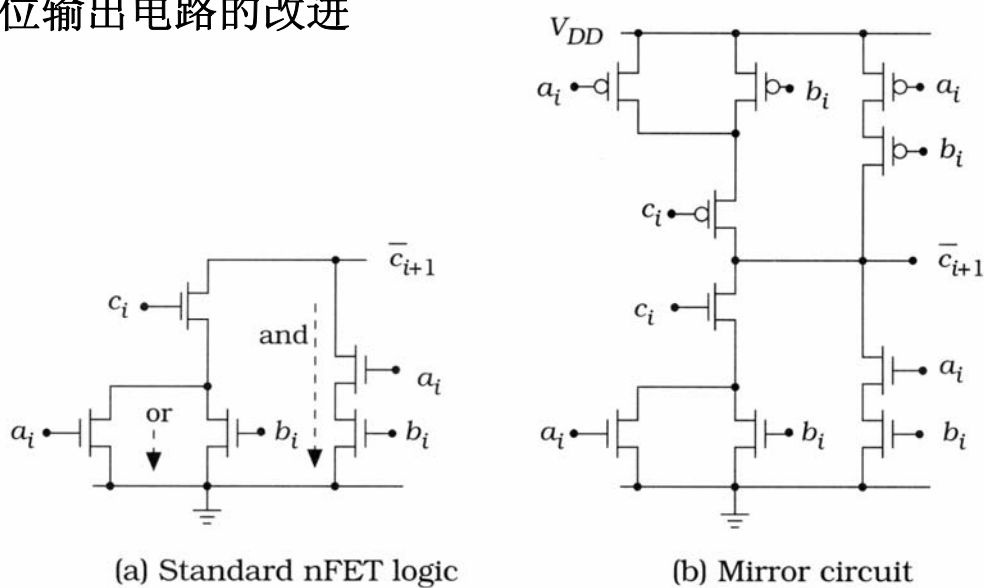


Figure 12.8 Evolution of carry-out circuit

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§ 12.1 一位加法器电路



镜像AOI实现的CMOS全加器

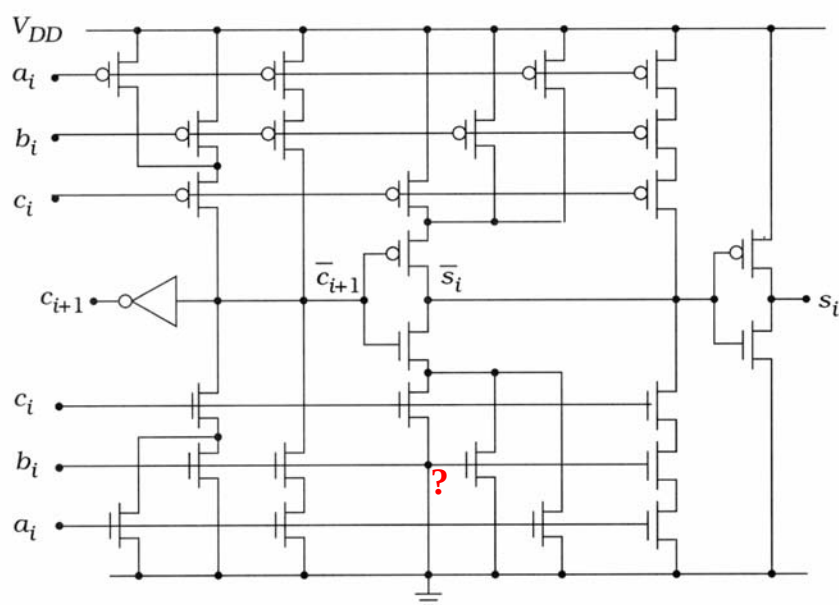


Figure 12.9 Mirror AOI CMOS full-adder

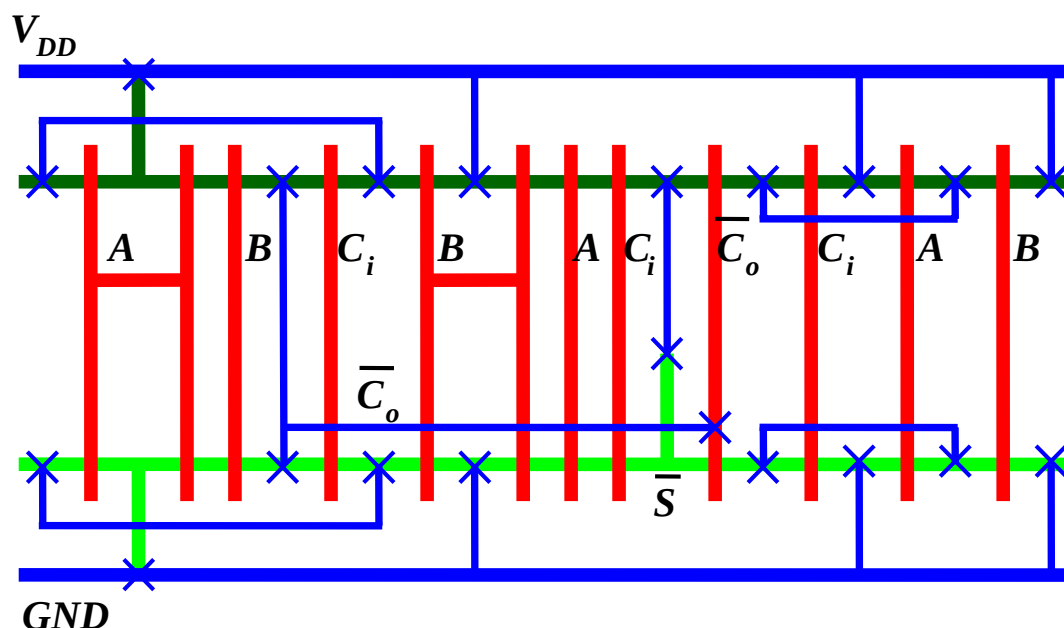
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§ 12.1 一位加法器电路

镜像加法器棍图



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§ 12.1 一位加法器电路

(2) 传输门实现的全加器电路

$$s_i = a_i \oplus b_i \oplus c_i$$

$$= (\overline{a_i \oplus b_i}) \cdot c_i + (a_i \oplus b_i) \cdot \overline{c_i}$$

$$c_{i+1} = a_i \cdot b_i + c_i \cdot (a_i \oplus b_i)$$

$$= (a_i \oplus b_i) \cdot c_i + (\overline{a_i \oplus b_i}) \cdot a_i$$

只需20个MOSFET

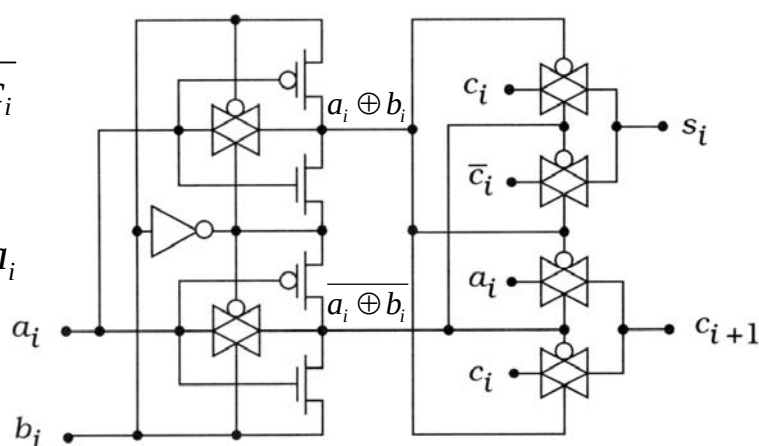


Figure 12.10 Transmission-gate full-adder circuit

电路特点: s_i 和 c_{i+1} 的延时几乎完全相同

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§ 12.1 一位加法器电路

(3) 双轨互补传输管逻辑 (CPL) 全加器设计

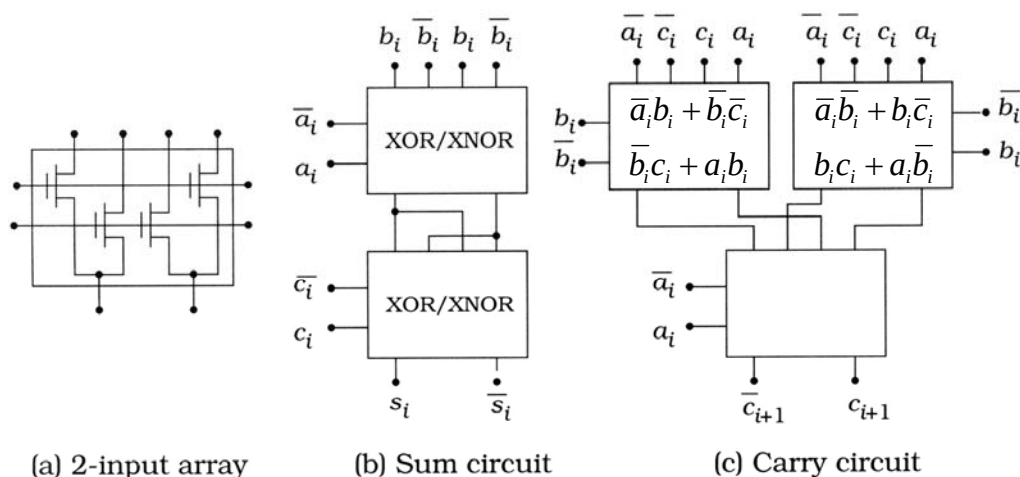


Figure 12.5 CPL full-adder design

$$s_i = a_i \oplus b_i \oplus c_i = (\overline{a_i \oplus b_i}) \cdot c_i + (a_i \oplus b_i) \cdot \overline{c_i}$$

$$c_{i+1} = a_i \cdot b_i + c_i \cdot (a_i \oplus b_i)$$

§ 12.2 串行进位加法器

4位串行进位加法器

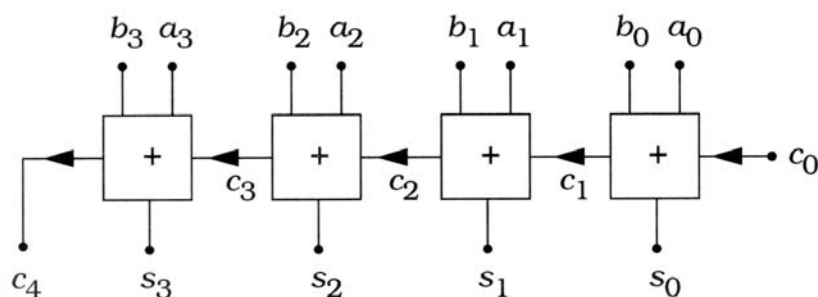


Figure 12.12 A 4-bit ripple-carry adder

§ 12.2 串行进位加法器

通过4位串行加法器最坏情形下的延迟

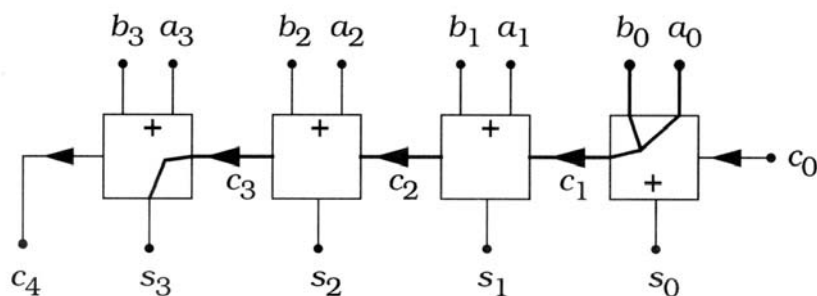


Figure 12.13 Worst-case delay through the 4-bit ripple adder

$$t_{4b} = t_{d3} + t_{d2} + t_{d1} + t_{d0}$$

$$t_{4b} = t_d(c_{in} \rightarrow s_3) + 2t_d(c_{in} \rightarrow c_{out}) + t_d(a_0, b_0 \rightarrow c_1)$$

推广:

$$t_{n-bit} = t_d(c_{in} \rightarrow s_{n-1}) + (n-2)t_d(c_{in} \rightarrow c_{out}) + t_d(a_0, b_0 \rightarrow c_1)$$

§ 12.3 超前进位加法器

超前进位算法的基础

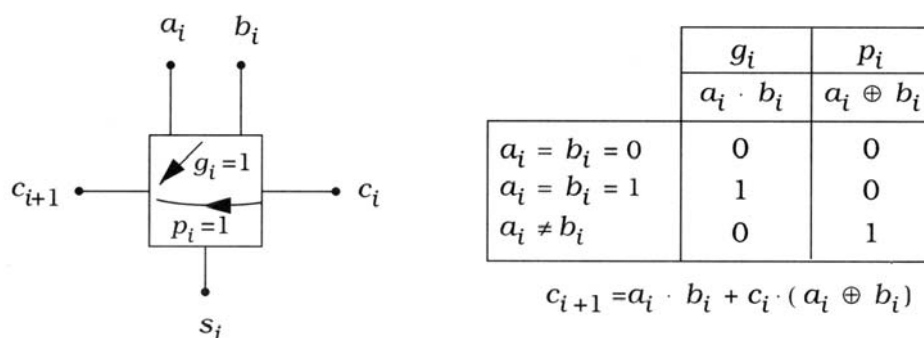


Figure 12.15 Basis of the carry look-ahead algorithm

$$c_{i+1} = a_i \cdot b_i + c_i \cdot (a_i \oplus b_i) \quad s_i = a_i \oplus b_i \oplus c_i$$

进位产生信号: $g_i = a_i \cdot b_i$

进位传播信号: $p_i = a_i \oplus b_i$

$$c_{i+1} = g_i + p_i \cdot c_i \quad s_i = p_i \oplus c_i$$

§ 12.3 超前进位加法器

超前进位算法的基础

$$c_{i+1} = g_i + p_i \cdot c_i \quad s_i = p_i \oplus c_i$$

$$c_1 = g_0 + p_0 \cdot c_0 \quad c_2 = g_1 + p_1 \cdot c_1$$

$$c_3 = g_2 + p_2 \cdot c_2 \quad c_4 = g_3 + p_3 \cdot c_3$$

$$c_2 = g_1 + p_1 \cdot (g_0 + p_0 \cdot c_0) = g_1 + p_1 \cdot g_0 + p_1 \cdot p_0 \cdot c_0$$

$$\begin{aligned} c_3 &= g_2 + p_2 \cdot (g_1 + p_1 \cdot g_0 + p_1 \cdot p_0 \cdot c_0) \\ &= g_2 + p_2 \cdot g_1 + p_2 \cdot p_1 \cdot g_0 + p_2 \cdot p_1 \cdot p_0 \cdot c_0 \end{aligned}$$

$$\begin{aligned} c_4 &= g_3 + p_3 \cdot (g_2 + p_2 \cdot g_1 + p_2 \cdot p_1 \cdot g_0 + p_2 \cdot p_1 \cdot p_0 \cdot c_0) \\ &= g_3 + p_3 \cdot g_2 + p_3 \cdot p_2 \cdot g_1 + p_3 \cdot p_2 \cdot p_1 \cdot g_0 + p_3 \cdot p_2 \cdot p_1 \cdot p_0 \cdot c_0 \end{aligned}$$

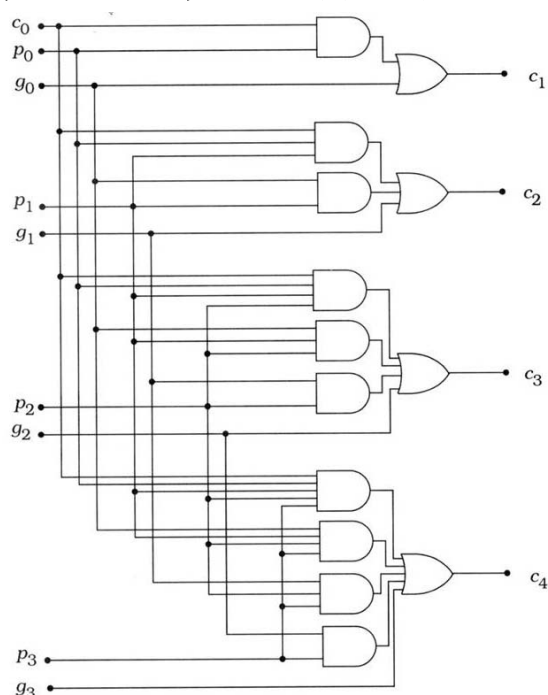
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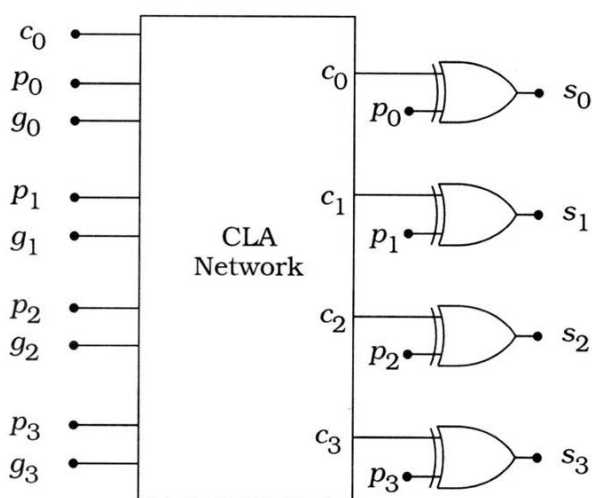
§ 12.3 超前进位加法器

4位CLA进位的逻辑电路



用CLA进位电路计算和

$$s_i = p_i \oplus c_i$$



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§ 12.3 超前进位加法器



实现CLA各项
进位的nFET
逻辑阵列

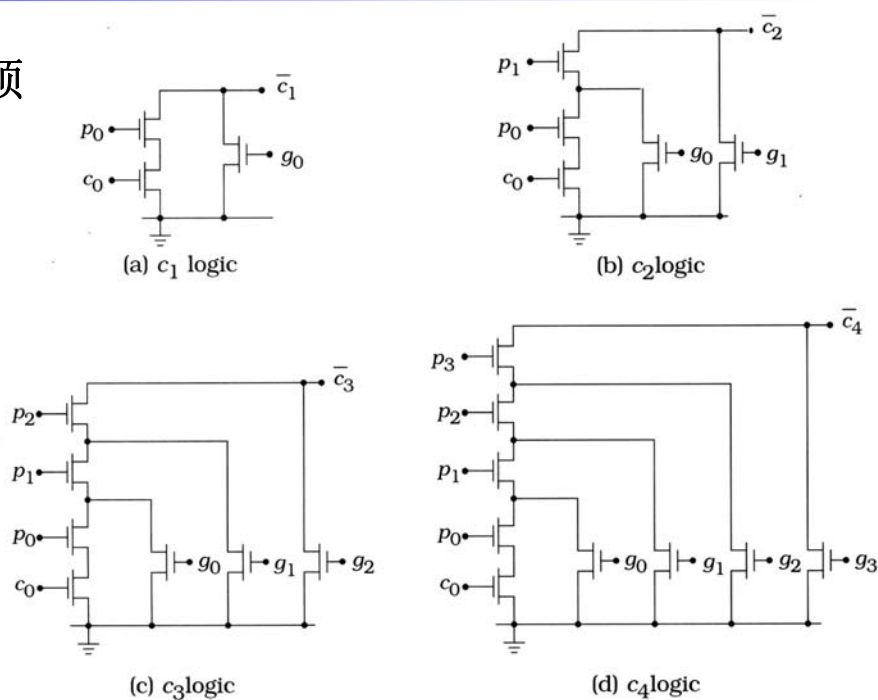


Figure 12.18 nFET logic arrays for the CLA terms

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§ 12.3 超前进位加法器



可能采用的三种电路

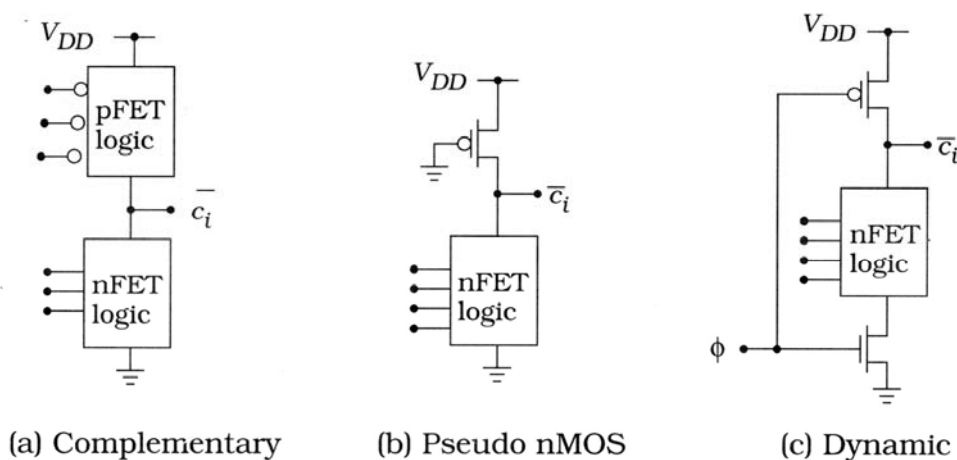


Figure 12.19 Possible uses of the nFET logic arrays in Figure 12.18

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§ 12.3 超前进位加法器



静态CLA镜像电路

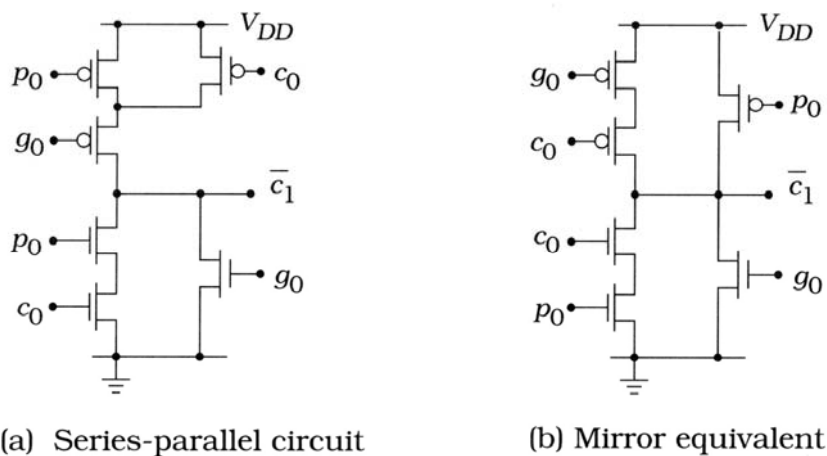


Figure 12.20 Static CLA mirror circuit

$$c_1 = g_0 + p_0 \cdot c_0$$

§ 12.3 超前进位加法器



产生 $\bar{c}_2$ 的静态镜像电路

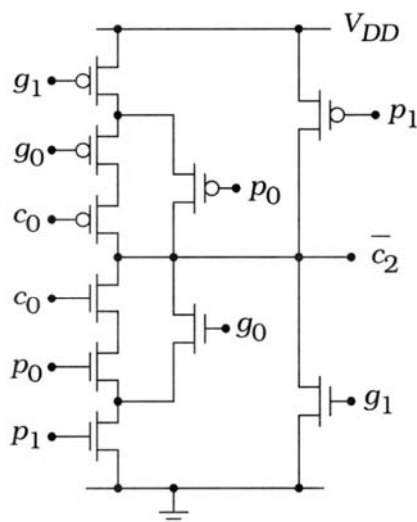


Figure 12.21 Static mirror circuit for $\bar{c}_2$

$$c_1 = g_0 + p_0 \cdot c_0$$

$$c_2 = g_1 + p_1 \cdot c_1 = g_1 + p_1(g_0 + p_0 \cdot c_0)$$

§ 12.3 超前进位加法器

MODL进位电路

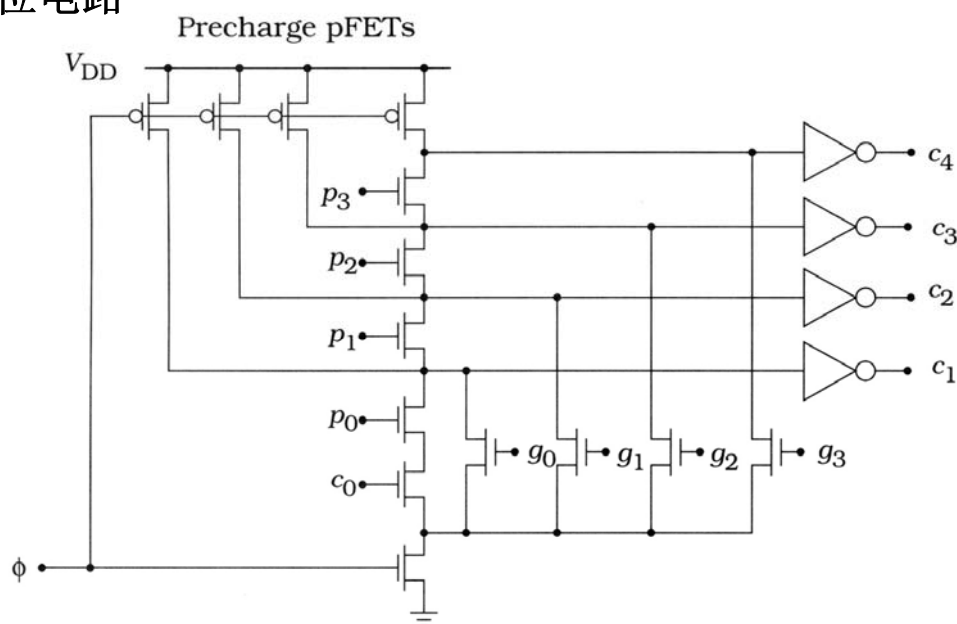


Figure 12.22 MODL carry circuit

§ 12.3 超前进位加法器

12.3.1 曼彻斯特进位链

$$c_{i+1} = g_i + p_i \cdot c_i$$

a_i	b_i	p_i	g_i	k_i
0	0	0	0	1
0	1	1	0	0
1	0	1	0	0
1	1	0	1	0

Figure 12.23 Propagate, generate, and carry-kill values

进位产生信号: $g_i = a_i \cdot b_i$

进位传播信号: $p_i = a_i \oplus b_i$

进位清除信号: $k_i = \overline{a_i + b_i} = \overline{a_i} \cdot \overline{b_i}$

§ 12.3 超前进位加法器



进位输出的开关电路

a_i	b_i	p_i	g_i	k_i
0	0	0	0	1
0	1	1	0	0
1	0	1	0	0
1	1	0	1	0

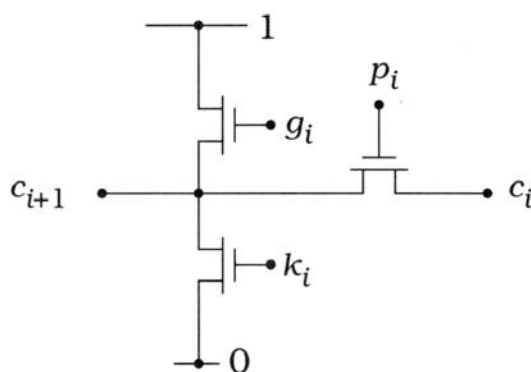


Figure 12.24 Switching network for the carry-out equation

进位产生信号: $g_i = a_i \cdot b_i$

进位传播信号: $p_i = a_i \oplus b_i$

进位清除信号: $k_i = \overline{a_i + b_i} = \overline{a_i} \cdot \overline{b_i}$

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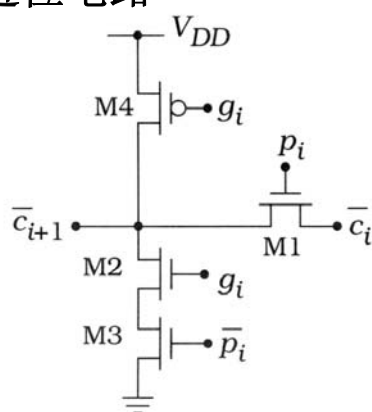
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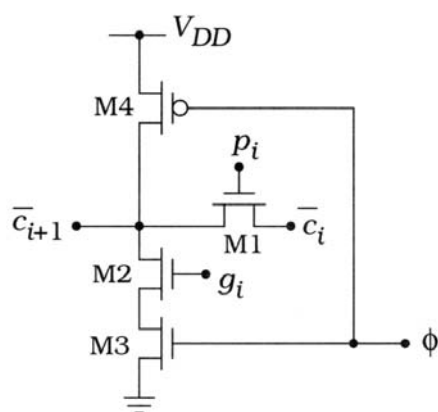
§ 12.3 超前进位加法器



曼彻斯特进位电路



(a) Static circuit



(b) Dynamic circuit

Figure 12.25 Manchester circuit styles

进位产生信号: $g_i = a_i \cdot b_i$ 进位传播信号: $p_i = a_i \oplus b_i$

进位清除信号: $k_i = \overline{a_i + b_i} = \overline{a_i} \cdot \overline{b_i}$

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§ 12.3 超前进位加法器



动态曼彻斯特进位链

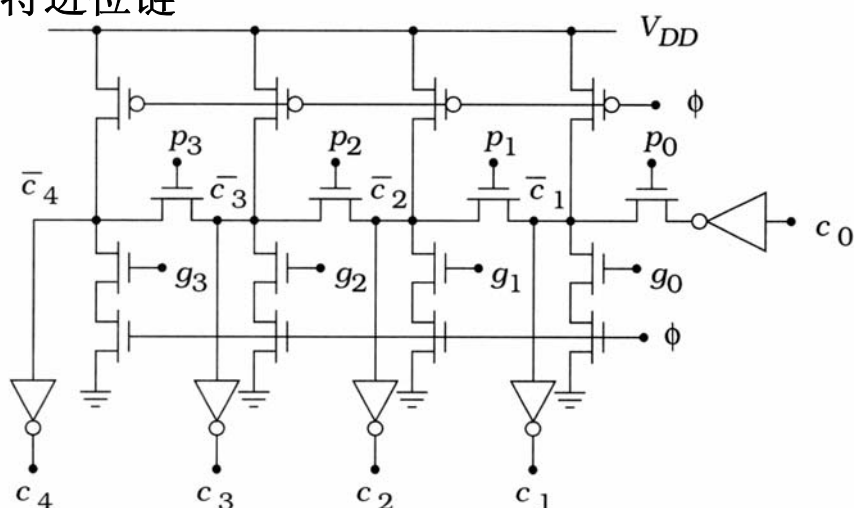


Figure 12.26 Dynamic Manchester carry chain

8位的加法器:进位输出 c_8 含有一项

$$p_7 \cdot p_6 \cdot p_5 \cdot p_4 \cdot p_3 \cdot p_2 \cdot p_1 \cdot p_0 \cdot c_0$$

§ 12.3 超前进位加法器



12.3.2 扩展为宽位加法器

n 位加法器电路

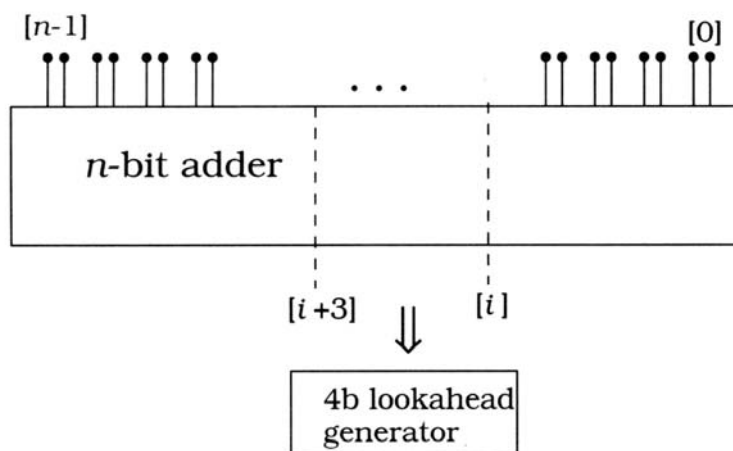


Figure 12.27 An n -bit adder network

§ 12.3 超前进位加法器



4位超前进位产生电路的信号

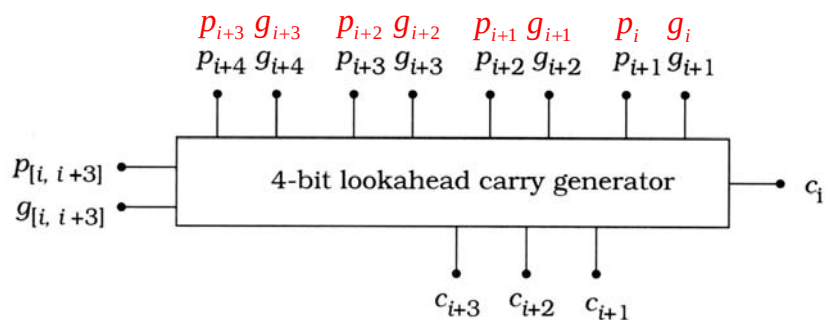


Figure 12.28 4-bit lookahead carry generator signals

块产生信号 $g_{[i,i+3]}$

$$g_{[i,i+3]} = g_{i+3} + p_{i+3} \cdot g_{i+2} + p_{i+3} p_{i+2} g_{i+1} + p_{i+3} p_{i+2} p_{i+1} g_i$$

块传播信号 $p_{[i,i+3]}$

$$p_{[i,i+3]} = p_{i+3} \cdot p_{i+2} \cdot p_{i+1} \cdot p_i$$

§ 12.3 超前进位加法器



块超前进位产生逻辑

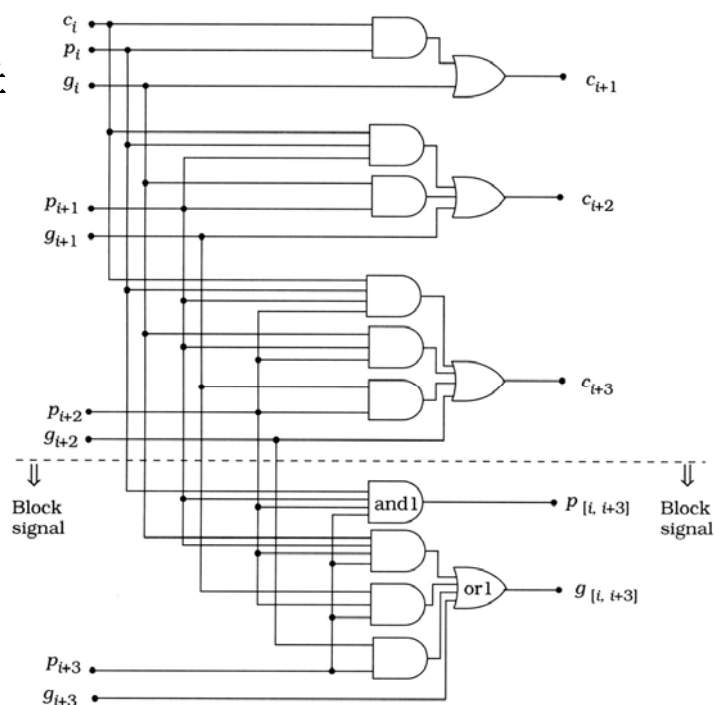


Figure 12.29 Block lookahead generator logic

§ 12.3 超前进位加法器

一个16位加法器的多层CLA块技术

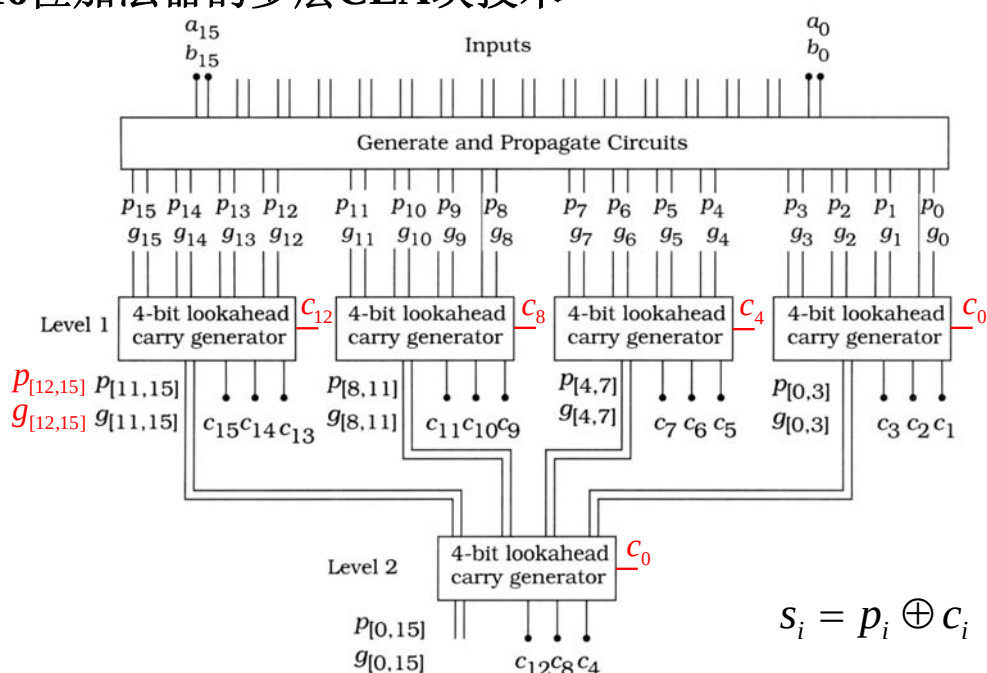


Figure 12.30 Multilevel CLA block scheme for a 16-bit adder

§ 12.3 超前进位加法器

64位CLA加法器的结构

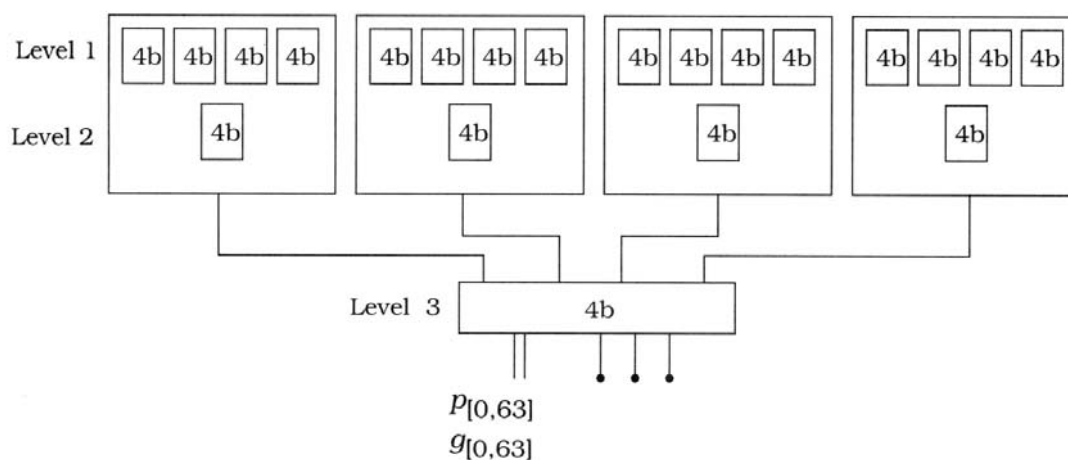


Figure 12.31 64-bit CLA adder architecture